THE STATIC OPTIMIZATION TASK OF OPTIMAL DESIGN OF NONLINEAR ELECTRONIC SCHEME

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The article deals with such an important selection of the elements of electronic scheme of the given configuration, when the certain requirements of technical task are satisfied and at the same time the selected optimality criteria reach the extreme value. The gives task has been solved by the method of one-criterion optimization, in particular, the method of center gravity. To formalize the given scheme we have compiled a mathematical model of optimization, which considers the requirements of technical task. The optimal design task of the presented electronic scheme was brought to the task of multi criteria optimization. The computational experiments have been resulted in the Pareto-optimal solutions, from which there was selected a compromise on that corresponds to the minimum capacity, required by the scheme. According to the optimal values of resistors, we have conducted a computerized analysis of the transient process of the given electronic scheme with the help of a computer program Electronics Workbench.

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1. INTRODUCTION

Optimization theory has recently been intensively developing and, therefore, contributes to the achievements of computing techniques. The increasing interest in complex (multidimensioanl, non-linear, nonrelational, multi-modal) tasks in engineering practice of modern technical systems of design and control, requires the need to develop effective methods of optimization, i.e. the need for synthesis of such methods, which easily, simply, fast and with a small expenditure of computer time provide the solution of extreme tasks for the purpose of their use in automated design systems.

The optimal control is more widely used in modern industry. One of the main practical directions of solving the optimal control tasks is a development of numerical methods.

2. THE TASK

It is necessary to find those values of elements of the electronic scheme configuration (in particular, the E-governance diagnostic electronic control scheme) in which the specific requirements of the technical task are satisfied and the criteria, chosen for optimum, reach extreme significance. In mathematical terms, the mentioned task is generally a multi-criterion optimization task and it is written as follows:

$$\begin{aligned}\min\{f(x)|g_i(x) \le 0, i=\overline{1,m};\\ a_j \le x_j \le b_j, j=\overline{1,n}\},\end{aligned} \tag{1}$$

where $f(x) = \left(f_1(x), f_2(x), ..., f_k(x)\right)$ is a target vector function, while $g_i(x)$ are linear or non-linear restrictions that define some set Ω of permissible solutions, while a_j and b_j are the values of optimization variables characterized by the range of possible modifications.

In multi-criterion tasks, the best solution of the possible ones is the subject that is fully responsible for the decision taken. Generally, a decision-maker is interested in receiving all the possible minimal values of (1) the criteria $f_1(x), f_2(x), ..., f_k(x)$ in the task as minimal as possible. In this case, the best (ideal) decision is the one that simultaneously minimizes all the above criteria on the set Ω. Unfortunately, similar solutions are not found in ordinary life. So, as a rule, we are dealing with compromise solutions that are called pareto-optimal solutions [1]. As there is no apriori information about the admissible solutions of the set Ω and the convection (conjugation) of the components of vector-function $f(x)$ in the multi-criterion optimization (1) task, therefore, the pareto-optical solution of the task can be determined by minimizing the following image:

$$\min_{x\in\Omega} \tilde{f}(x) = \min_{x\in\Omega} \max_{i=1,2,...,k} \lambda_i f_i(x), \tag{2}$$

where λ_i real numbers that satisfy the condition $\lambda_i, >0, i=1,2,...,k \sum_{i=1}^{k} \lambda_i = 1$. In this case, the following algorithmic scheme can be used to find one pareto-optimal solution:

1. The arbitrarily chosen values of λ_i coefficients, used to fulfill the condition: $\lambda_1 + \lambda_2 + ... + \lambda_k = 1$.

2. The values of $f(x)$ vector-function components are calculated: $y_i(x) = \lambda_i f_i(x), i = 1, 2, ..., k$.

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3. The second component of maximum importance will be chosen among the components, computed by the vector-function: $\tilde{f}(x) = \max\limits_{i=1,2,\ldots,k} \lambda_i f_i(x)$.

4. The following task of a single criterion minimization will be solved:

$$\min_{x\in\Omega} \left\{ \tilde{f}(x) | x \in \Omega \subset R^n \right\} . \qquad (3)$$

A method of one criterion optimization, in particular, the method of gravity centers [2] can be used to solve the task. The obtained minimum represents the compromise solution of the multi-criterion optimization task (1). The pareto-optimal solutions of N quantity is determined by the repetition of N quantity of 10...40 procedures, the best option of which is chosen by a decision-maker.

The scheme for solution of multi-criterion optimization tasks is used in the optimal design tasks of non-linear electronic schemes in the case if the latter is brought to the optimization model (1).

As an example we have used the electronic principle scheme of designed object, which is used for a adress decoder control in memory device (Fig.1) [3]. A mathematical model of optimization has been introduced for the formalization purposes; the model takes into consideration the following requirements of the technical task [4]:

1) The scheme should work reliably in a wide range of temperature:$-60°\mathrm{C} \le t \le +125°\mathrm{C}$;

2) The minimum level of input signal (logical "0") should be no more than +0.4 Volts;

3) The maximum level of input signal (logical "1") should be no less than +2.4 Volts;

4) The minimum level of output signal is no more than +0.4 Volts;

5) The maximum level of output signal is no less than +2.4 Volts;

6) The average time of output signal delay is not more than 40 nanoseconds;

7) The capacity required by the scheme in the static mode is not more than 40 mV.

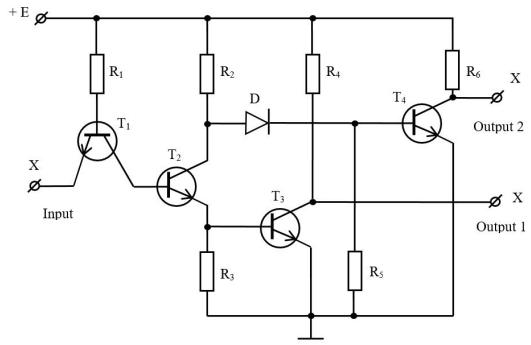

Fig.1. *A adress decoder control scheme in memory device*

In order to simplify the mathematical model, let's use a linear models of transistor and diode[5] instead of nonlinear models of active elements, and draw equivalent schemes that correspond to two static conditions of the given scheme:

- H condition, when a signal (logical "0") of the scheme is lower than the input one (Fig.2);

- B condition, when a signal (logical "1") of the scheme is higher than the input one (Fig.3). Since this scheme has two conditions, the static power is defined as the mean arithmetic of conditions and:

$$P = 0.5(P^0 + P^1) . \qquad (4)$$

The power, consumed in the H condition by the scheme, is:

$$P^0 = (J_1^0 + J_2^0 + J_3^0)E , \qquad (5)$$

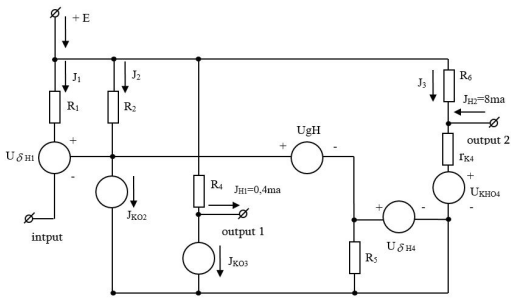

Fig.2. *H condition when a low signal (logical "0") on the introductory scheme is supplied*

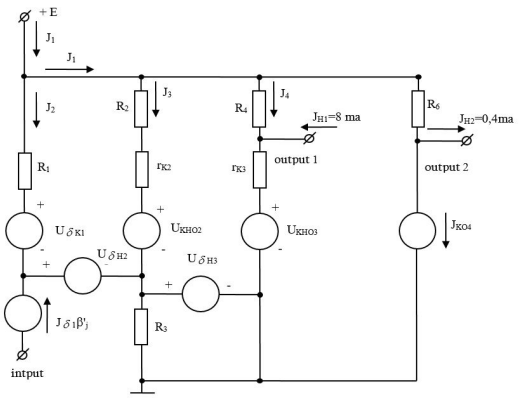

Fig.3. *B condition when a high signal (logical "1") is supplied to the intrusion circuits*

where E is a supply voltage, while

$$J_1^0 = \frac{E - U_{\delta H1} - U_{\text{input}}}{R_1}\,, \tag{6}$$

$$J_2^0 = \frac{E - U_{\delta H4} - U_{gH} - J_{k02}R_2}{R_2}\,, \tag{7}$$

$$J_3^0 = \frac{E - U_{KHO4}}{R_6 + r_{K4}}\,, \tag{8}$$

where $U_{\delta H1}$ and $U_{\delta H4}$ are correspondingly T_1 and T_4 transistors voltage slips in the mode of intersection of emitter bases; the strength of the power of the abscess of J_{k02} – T_2 transistors in the loop mode; U_{KHO4} – input voltage; r_{K4} – T_4 transistor collector's impedance.

Putting J_1^0, J_2^0 and J_3^0 values in expression (5) we receive:

$$\begin{aligned} P^0 = \Bigg(&\frac{E - U_{\delta H1} - U_{\text{input}}}{R_1} + \\ &+ \frac{E - U_{\delta H4} - U_{gH} - J_{k02}R_2}{R_2} + \\ &+ \frac{E - U_{KHO4}}{R_6 + r_{K4}}\Bigg) E\,. \end{aligned} \tag{9}$$

The transistor T_4 operates in the saturated mode in H condition, what can be represented by expression [6]:

$$\frac{\beta_4 J_{\delta 4}}{J_{KH4}} \geq S\,, \tag{10}$$

where the static coefficient $J_{\delta 4}$ of strengthening the transistor β_4 is a base current power in the saturated mode; J_{KH4} – the correction current power of the saturated transistor; S – the coefficient of saturation, $S = 1.2$.

Let's determine $J_{\delta 4}$ and J_{KH4} of the transistor T_4:

$$\begin{aligned} J_{\delta 4} &= J_2 - \frac{U_{\delta H4}}{R_5} = \\ &= \frac{E - U_{\delta H4} - U_{gH} - J_{KO2}R_2}{R_2} - \frac{U_{\delta H4}}{R_5}\,, \end{aligned} \tag{11}$$

$$J_{KH4} = J_3 + J_{\Gamma 2}^0 = \frac{E - U_{KHO4}}{R_6 + r_{K4}} + J_{G2}^0\,, \tag{12}$$

where $J_{G2}^0 = 8$ is the equivalent generator of milliamper current power. By inserting the last data in the expression (10), we get the condition of T_4 transistor saturation:

$$\frac{\beta_4 \left(\frac{E - U_{gH} - U_{\delta H4} - J_{KO2}R_2}{R_2} - \frac{U_{\delta H4}}{R_5}\right)}{\frac{E - U_{KHO4}}{R_6 + r_{k4}} + 8} \geq 1.2\,. \tag{13}$$

Besides the technical requirements, the normal operation of the loading scheme needs to maintain certain levels of output voltage. Therefore, the conditions considering these limitations are as follows:

$$U_{\text{output1}} = E - \left(J_{G1}^0 + J_{KO3}\right) R_4 \geq 2.4\,, \tag{14}$$

$$U_{\text{output2}} = U_{KHO4} + \left(J_{\Gamma 2}^0 + \frac{E - U_{KHO4}}{R_6 + r_{K4}}\right) r_{K4} \leq 0.4\,, \tag{15}$$

where $J_{G1}^0 = 0.4$ milliampere.

The power required by the scheme in condition B can be determined similarly to the expression (5):

$$P^1 = \left(J_2^1 + J_3^1 + J_4^1\right) E\,, \tag{16}$$

$$J_2^1 = \frac{E - U_{\delta K1} - U_{\delta H2} - U_{\delta H3}}{R_1}\,, \tag{17}$$

$$J_3^1 = \frac{E - U_{KHO2} - U_{\delta H3}}{R_2 + r_{K2}}\,, \tag{18}$$

$$J_4^1 = \frac{E - U_{KHO3}}{R_4 + r_{K3}}\,, \tag{19}$$

where $U_{\delta K1}$ is a voltage drop on the base-collector's transition of the transistor T_1; correspondingly,$U_{\delta H2}$ and $U_{\delta H3}$ are the voltage drops on the intersection of emitter bases of the saturated transistor T_2 and T_3; r_{K2} and r_{K3} – are correspondingly T_2 and T_3 transistors' collector interference.

Putting J_2^1, J_3^1 and J_4^1 values in the expression (16) we obtain:

$$\begin{aligned} P^1 = \Bigg(&\frac{E - U_{\delta K1} - U_{\delta H2} - U_{\delta H3}}{R_1} + \\ &+ \frac{E - U_{KHO2} - U_{\delta H3}}{R_2 + r_{K2}} + \\ &+ \frac{E - U_{KHO3}}{R_4 + r_{K3}}\Bigg) E\,. \end{aligned} \tag{20}$$

The transistors T_2 and T_3 in condition B are saturated, therefore, the conditions of saturation are expressed as follows:

$$\frac{\beta_2 J_{\delta 2}}{J_{KH2}} \le 1.2, \frac{\beta_3 J_{\delta 3}}{J_{KH3}} \le 1.2\,. \tag{21}$$

The equivalent scheme determines:

$$J_{\delta 2} = J_{K1} = J_{\delta 1}(1+\beta_i) = J_2(1+\beta_i) = \\ = \frac{E - U_{\delta K1} - U_{\delta H2} - U_{\delta H3}}{R_1}(1+\beta_i)\,, \tag{22}$$

$$J_{KH2} = J_3 = \frac{E - U_{KHO2} - U_{\delta H3}}{R_2 + r_{K2}}\,, \tag{23}$$

$$J_{\delta 3} = J_{\delta 2} + J_{KH2} - \frac{U_{\delta H3}}{R_3} = \\ = \frac{E - U_{\delta K1} - U_{\delta H2} - U_{\delta H3}}{R_1}(1+\beta_i) + \\ + \frac{E - U_{KHO2} - U_{\delta H3}}{R_2 + r_{K2}} - \frac{U_{\delta H3}}{R_3}\,, \tag{24}$$

$$J_{KH3} = \frac{E - U_{KHO3}}{R_4 + r_{K3}} + J^1_{G1}\,, \tag{25}$$

where β'_i is an invertion coefficient of strengthening the transistor T_1, while $J^1_{G1} = 8$ milliampere.

The result of inserting the latest data in the expression (21) is:

$$\frac{\beta_2 \frac{E - U_{\delta K1} - U_{\delta H2} - U_{\delta H3}}{R_1}(1+\beta_i)}{\frac{E - U_{KHO2} - U_{\delta H3}}{R_2 + r_{K2}}} \ge 1.2\,, \tag{26}$$

$$\frac{\beta_3 \left[\frac{E - U_{\delta K1} - U_{\delta H2} - U_{\delta H3}}{R_1}(1+\beta_i) + \right.}{\frac{E - U_{KHO3}}{R_4 + r_{K3}} + 8} \\ \left. + \frac{E - U_{KHO2} - U_{\delta H3}}{R_2 + r_{K2}} - \frac{U_{\delta H3}}{R_3}\right] \\ \frac{}{\frac{E - U_{KHO3}}{R_4 + r_{K3}} + 8} \ge 1.2\,. \tag{27}$$

The conditions for maintaining the output signals at certain levels in B condition are similar to the expresswions (14) and (15):

$$U_{\text{output1}} = U_{KHO3} + \left(J^1_{G1} + \right. \\ \left. + \frac{E - U_{KHO3}}{R_4 + r_{K3}}\right) r_{K3} \le 0.4\,, \tag{28}$$

$$U_{\text{output2}} = E - \left(J^1_{G2} + J_{KO4}\right) R6 \ge 2.4\,, \tag{29}$$

where $J^1_{G2} = 0.8$ milliampere.

Putting the expressions (9) and (20) in the (4) one, we receive an analytical expression of the power consumed by the scheme in static mode:

$$P = 0.5\left(\frac{E - U_{\delta H1} - U_{\text{input}}}{R_1} + \right. \\ + \frac{E - U_{\delta H4} - U_{gH} - J_{k02}R_2}{R_2} + \\ + \frac{E - U_{KHO4}}{R_6 + r_{K4}} + \\ + \frac{E - U_{\delta K1} - U_{\delta H2} - U_{\delta H3}}{R_1} + \\ \left. + \frac{E - U_{KHO2} - U_{\delta H3}}{R_2 + r_{K2}} + \frac{E - U_{KHO3}}{R_4 + r_{K3}}\right) E\,. \tag{30}$$

As it is known, the basic characteristic of nonlinear schemes' work in impulsive mode is the time of switching delay, which is defined as the average time of front and rear fronts of the voltage signal:

$$t_{\text{delay}} = 0.5\,(t_1 + t_2)\ . \tag{31}$$

For the logic schemes the delay time t_1 of the leading front is defined as the difference between those periods of time when the input and output voltage signals reach 50% of their maximum level, and the delay time t_2 of the back front is determined as the difference between the moments of time when the input and output voltage signals are reduced by 50% of their maximum level.

The analytical calculation of t_{delay} is associated with great difficulties, because it requires solving a higher-order differential equation. Therefore, we used Taylor's formula for its calculation:

$$t_{\text{delay}} \approx \bar{t}_{\text{delay}} + \sum_{i=1}^{n} \frac{\partial t_{\text{delay}}}{\partial R_i}\left(R_i - \bar{R}_i\right)\ , \tag{32}$$

where $\bar{t}_{\text{delay}} = t_{\text{delay}}\left(R_1 = \bar{R}_1, R_2 = \bar{R}_2, ..., R_n = \bar{R}_n\right)$, and $\bar{R}_1, \bar{R}_2, ..., \bar{R}_n$ are any acceptable values of resistors.

Since this scheme has two options and there is the following approximate equation $\frac{\partial t_{\text{delay}}}{\partial R_i} \approx \frac{\Delta t_{\text{delay}}}{\Delta R_i}$ so we obtain:

$$t_{\text{delay1}} = \bar{t}_{\text{delay1}} + \\ + \sum_{i=1}^{6} \frac{\Delta t_{\text{delay1}}}{\Delta R_i}\left(R_i - \bar{R}_i\right) \le \tilde{t}_{\text{delay1}}\,, \tag{33}$$

$$t_{\text{delay2}} \approx \bar{t}_{\text{delay2}} + \\ + \sum_{i=1}^{6} \frac{\Delta t_{\text{delay2}}}{\Delta R_i}\left(R_i - \bar{R}_i\right) \le \tilde{t}_{\text{delay2}}\,, \tag{34}$$

where $\tilde{t}_{\text{delay1}}$ and $\tilde{t}_{\text{delay2}}$ are the boundary admissible values of the correspondig parametres.

$\frac{\Delta t_{\text{delay1}}}{\Delta R_i}$ and $\frac{\Delta t_{\text{delay2}}}{\Delta R_i}$ coefficients are defined on the basis of the experiment, by use of the electronic scheme analysis of any computer program. The results of the experiment are shown in Fig.1.

Putting the obtained results in expressions (31) and (32) we receive:

$$t_{delay1} = 28.62 - 0.2(R_2 - 3) + 0.525(R_3 - 2) + \\ + 3.76(R_4 - 2.4) \le \tilde{t}_{delay1}\,, \tag{35}$$

$$t_{delay2} = 36 - (R_1 - 4) + 3.333(R_2 - 3) + \\ + 0.7(R_5 - 5) + 5(R_6 - 2.4) \le \tilde{t}_{delay}\,. \tag{36}$$

Independent variables in the above expressions are the passive elements of the scheme: R_1, R_2, R_3, R_4, R_5 and R_6, which possible change range of values is limited by schematic concepts:

$$1.0\,k\Omega \le R_i \le 5.0\,k\Omega,\ \ i = \overline{1...6}\,. \tag{37}$$

The values of the transistor collective power forces are limited as well. For example, the maximally acceptable value of a collector current power capacity of T_2 transistor is 3 milliampere, while T_3 and T_4 transistors have 15 milliampers.

Table 1. *Experimental results*

No	R_1 $k\Omega$	R_2 $k\Omega$	R_3 $k\Omega$	R_4 $k\Omega$	R_5 $k\Omega$	R_6 $k\Omega$	Δt_{delay1} Nsec	Δt_{delay2} Nsec	$\frac{\Delta t_{\text{delay1}}}{\Delta R_i}$	$\frac{\Delta t_{\text{delay2}}}{\Delta R_i}$
1	4.0	3.0	2.0	2.4	5.0	2.4	28.62	36.0	-	-
2	4.8	3.0	2.0	2.4	5.0	2.4	28.62	35.2	0	-1.0
3	4.0	3.6	2.0	2.4	5.0	2.4	28.50	38.0	-0.2	3.333
4	4.0	3.0	2.4	2.4	5.0	2.4	28.83	0	0.525	0
5	4.0	3.0	2.0	2.9	5.0	2.4	30.50	0	3.76	0
6	4.0	3.0	2.0	2.4	6.0	2.4	28.62	36.7	0	0.7
7	4.0	3.0	2.0	2.4	5.0	2.9	28.62	38.5	0	5.0

In order to evaluate the normal functioning of the scheme in the given temperature, it is necessary to use the margin test method, according to which the scheme capability is determined by the worst values of the input parameters and external conditions.

Taking into account the numerical value of the electrical-physical parameters of the active elements and the margin test results, as well as the above obtained correlations, we have identified the following optimized mathematical model of the designed electronic scheme:

$$f_1(R_1,R_2,...,R_6)=P=\frac{19.55}{R_1}+\frac{12.3}{R_2+0.011}+ +\frac{15.0}{R_4+0.005}+\frac{9.63}{R_2}+\frac{15.0}{R_6+0.005}, \tag{38}$$

$$f_2(R_1,R_2,...,R_6)=t_{delay}=5R_6+ +0.7R_5+3.333R_2-R_1+14.501, \tag{39}$$

$$\frac{(R_4+0.005)\,[R_3(48.3R_1+23.4R_2+0.2574)- -R_1(14R_2+0.154)]}{R_1R_3(R_2+0.011)(8R_4+4.49)}\geq 12, \tag{40}$$

$$\frac{7.3R_2+0.0803}{R_1}\geq 1.2, \tag{41}$$

$$\frac{(R_6+0.005)(35.4R_5-14R_2)}{R_2R_5(8R_6+4.49)}\geq 12, \tag{42}$$

$$\frac{4.8}{R_2+0.017}\leq 3, \tag{43}$$

$$\frac{8R_4+5.49}{R_4+0.005}\leq 15, \tag{44}$$

$$\frac{8R_6+5.49}{R_6+0.005}\leq 15, \tag{45}$$

$$0.8R_4\leq 2.1, \tag{46}$$

$$0.8R_6\leq 2.1, \tag{47}$$

$$\frac{0.114R_4+0.044912}{R_4+0.008}\leq 0.4, \tag{48}$$

$$\frac{0.114R_6+0.044912}{R_6+0.008}\leq 0.4, \tag{49}$$

$$3.76R_4+0.525R_3-0.2R_2+19.146\leq 40, \tag{50}$$

$$\frac{23.6}{R_1}+\frac{13.3}{R_2+0.017}+\frac{12.3}{R_4+0.008}+ +\frac{11.7}{R_2}+\frac{12.3}{R_6+0.008}\leq 40, \tag{51}$$

$$0\leq |R_4-R_6|\leq 0.01, \tag{52}$$

$$1.0\leq R_i\leq 5.0, i=\overline{1,6}. \tag{53}$$

In the inequation system (52), the restriction is imposed by R4 and R6 interference to maintain the approximate equation: $R_4\approx R_6$.

Thus, the task of optimal design (38)–(53) of the electronic circuit has been brought to the task of multi-criterion optimization, and it is as follows: the values of the resistors R_1, R_2, R_3, R_4, R_5 and R_6 for which the static capacity (38) and the scheme switching delay time (39) achieve their minimum value of inequalities (40)–(53) at the time of scheme satisfaction.

3. RESULTS OF COMPUTATIONAL EXPERIMENT

The task of multi-criterion optimization (38)–(53) presented in the article has been developed by the processed software on the basis of the algorithmic scheme, which uses the method of gravity centers [6] to solve the tasks of a single criterion optimization. Table 2 represents the pareto-optical solutions obtained from computational experiments, among which there was selected that compromise solution, which corresponds to the minimum capacity required by the scheme: $P^*=f_1(R)=23.5106$ milliwatts and the scheme switching minimum time $t^*_{\text{delay}}=f_2(R)=22.9738$ nanoseconds. The values of private criteria are achieved in the following optimal values of resistors: $R_1^*=4.82\,k\Omega$, $R_2^*=2.01\,k\Omega$, $R_3^*=4.63\,k\Omega$, $R_4^*=1.12\,k\Omega$, $R_5^*=1.44\,k\Omega$, $R_6^*=1.12\,k\Omega$. According to the optimal values of resistors, the computer analysis [7] of the transition process of the electronic scheme was conducted by computer program Electronics Workbench, the results of which are presented in Fig.4. Using the algorithms and programs, developed in the paper, it is possible to solve the complex tasks of optimal design of electronic devices with the minimum waste of computer time and the acceptable accuracy.

Table 2. *Pareto-Optimal solutions received by computational experiment*

No	$\tilde{f}(R)$	$f_1(R)$	$f_2(R)$	R_i, $k\Omega$
1	10.3078	14.6096	35.0066	$R_1 = 4.35; R_2 = 3.41; R_3 = 3.39; R_4 = 2.30; R_5 = 2.84; R_6 = 2.30$
2	13.3837	13.4824	38.3939	$R_1 = 4.70; R_2 = 4.28; R_3 = 3.48; R_4 = 2.32; R_5 = 3.83; R_6 = 2.33$
3	10.1738	13.8741	37.0253	$R_1 = 4.58; R_2 = 3.95; R_3 = 2.74; R_4 = 2.30; R_5 = 3.43; R_6 = 2.31$
4	19.7741	20.2646	26.6166	$R_1 = 4.09; R_2 = 2.12; R_3 = 2.63; R_4 = 1.54; R_5 = 2.03; R_6 = 1.54$
5	17.6691	23.5106	22.9738	$R_1 = 4.82; R_2 = 2.01; R_3 = 4.63; R_4 = 1.12; R_5 = 1.44; R_6 = 1.12$
6	11.0872	16.5291	29.0072	$R_1 = 4.82; R_2 = 2.63; R_3 = 4.21; R_4 = 1.91; R_5 = 1.40; R_6 = 1.92$
7	21.2501	22.8014	25.9212	$R_1 = 4.01; R_2 = 2.29; R_3 = 4.08; R_4 = 1.19; R_5 = 2.62; R_6 = 1.19$

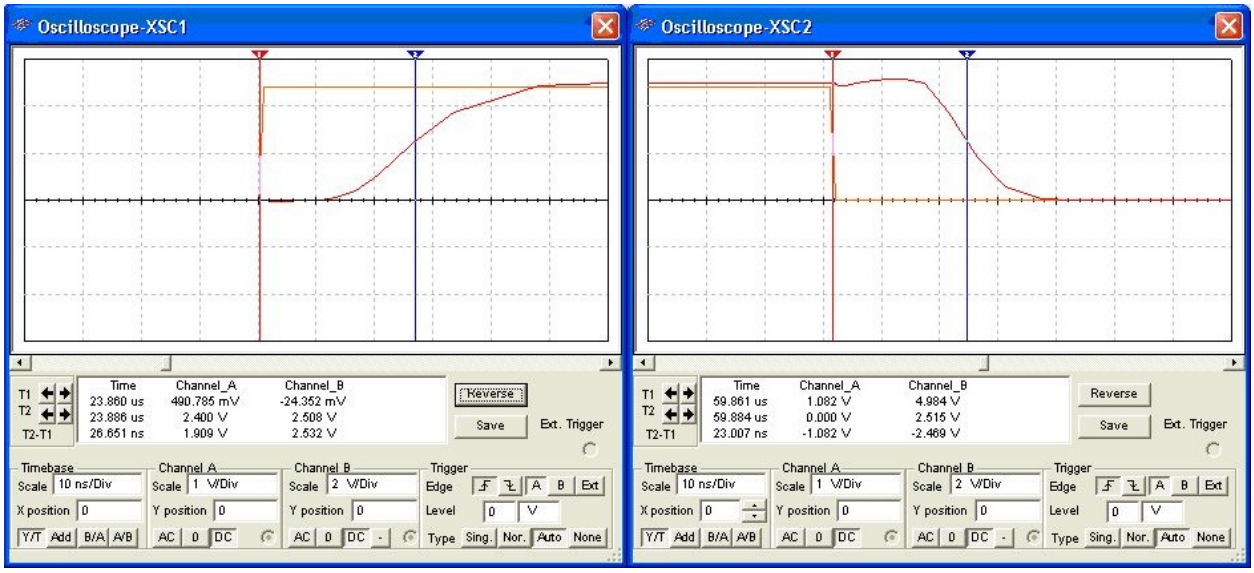

Fig.4. *Results of computer analysis of the transition process of the scheme discussed. The Figure shows that the experimental results are satisfactory and they are compatible with the theoretically calculated results with the acceptable accuracy*

4. SUMMARY

The article deals with the practical possibilities of the use of algorithms developed on the basis of gravity centers methodology in engineering design systems, in particular, in the automated system of optimal design of electronic devices, by solving concrete tasks of practical significance. Namely, there is represented a mathematical model of electronic control scheme for the address decoder used in the computer's memory device; the optimal parameters of the scheme passive elements are defined from the perspective of multi-criterion optimization and the developed algorithm.

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ЗАДАЧА СТАТИЧЕСКОЙ ОПТИМИЗАЦИИ ОПТИМАЛЬНОГО ДИЗАЙНА НЕЛИНЕЙНОЙ ЭЛЕКТРОННОЙ СХЕМЫ

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Рассматривается такой важный выбор элементов электронной схемы данной конфигурации, когда выполняются определенные требования технической задачи, и в то же время выбранные критерии оптимальности достигают экстремального значения. Задача решена методом однокритериальной оптимизации, в частности, методом центра тяжести. Для формализации данной схемы мы составили математическую модель оптимизации, в которой рассматриваются требования технической задачи. Задача оптимального дизайна данной электронной схемы была представлена в виде задачи многокритериальной оптимизации. Вычислительные эксперименты были проведены в Парето-оптимальных решениях, из которых был выбран компромисс, который соответствует минимальной емкости, требуемой схемой. В соответствии с оптимальными значениями резисторов мы провели компьютеризированный анализ переходного процесса данной электронной схемы с помощью компьютерной программы Electronics Workbench.

ЗАВДАННЯ СТАТИЧНОЇ ОПТИМІЗАЦІЇ ОПТИМАЛЬНОГО ДИЗАЙНУ НЕЛІНІЙНОЇ ЕЛЕКТРОННОЇ СХЕМИ

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Розглядається такий важливий вибір елементів електронної схеми заданої конфігурації, коли виконуються певні вимоги технічного завдання, і в той же час вибрані критерії оптимальності досягають крайнього значення. Завдання було вирішено методом однокритеріальної оптимізації, зокрема, методом центра тяжіння. Для формалізації даної схеми ми склали математичну модель оптимізації, яка розглядає вимоги технічного завдання. Задачу оптимального дизайну представленої електронної схеми було зведено до задачі багатокритеріальної оптимізації. Обчислювальні експерименти були отримані в Парето-оптимальних рішеннях, з яких був обраний компроміс, що відповідає мінімальній ємності, необхідній за схемою. Згідно з оптимальними значеннями резисторів ми провели комп'ютерний аналіз перехідного процесу даної електронної схеми за допомогою комп'ютерної програми Electronics Workbench.