Structure model of bistable current switching in CdS films

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The VCC of CdS films in static and dynamic modes have been measured. A number of new kinetic features has been revealed for the electrically stimulated switching between two stable states. The states differ in their electric conduction levels by a factor of 10^4 and are kept after the external power supply is switched off. A new structure model of the bistable switching has been proposed.

Измерены ВАХ пленок CdS в статическом и динамическом режимах. Обнаружен ряд новых особенностей кинетики электростимулированного переключения между двумя устойчивыми состояниями, которые отличаются по уровню электропроводности в 10^4 раз и сохраняются после отключения внешнего напряжения. Предложена новая структурная модель бистабильного переключения.

In many semiconductors, including CdS polycrystal films, the negative differential resistance (NDR) as well as bistable switching and memory effects, that is, the change of the material high-resistance (HR) to the low-resistance (LR) one and vice versa, are observed in many semiconductors, including CdS polycrystal films [1, 2]. Although the switching effects in an electric field are used widely in different automatic systems such as commutation devices, logic memory systems, ROMs, etc., there is no unique commonly accepted interpretation of the switching mechanism. This evidences the actuality of further investigation into that complex phenomenon associated with several simultaneous physical processes, namely, electric, thermal, diffusion, and phase structure ones.

Among numerous points of view presented in literature [3−6] concerning the switching effects, it is just the mechanism associated with structure and phase transformations [7] that is preferred in this work. The semiconducting films of A_2B_6 compounds are of a special interest in this connection. These films present a specific stacking morphology of grains consisting of thin plates comprising twins and polymorphous phases alternating along the normal to closely packed plans [8]. Perhaps there is a relation between the above-mentioned structure phenomena and electric ones. Taking the above into account, this work is aimed at the study of dynamic details of the switching and memory effects that might be useful to interpret structurally the kinetics of the phenomenon.

The VCC with S-shaped NDR, the reversible electric switching and memory effects in 1 to 2 μm thick CdS films were studied in experiment using a standard measuring device making it possible to obtain the VCC both in static and dynamic modes provided by little modifications in the measuring scheme (Fig. 1). Molybdenum and palladium point contacts were used at the samples. The voltage applied to the sample was controlled by resistor R_1. To control the ballast line, a the resistor R_n was used being varied within 1 to 10 kΩ range. A PC was used as the recorder. The signal taken off from the voltage divider R_3, R_4 ($R_4 > R_3$) was applied to the analog-to-digital coder of the PC and
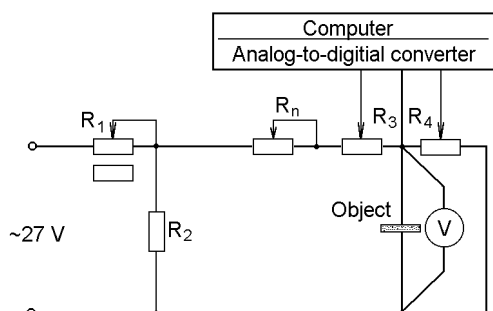
Fig. 1. Structure scheme of dynamic VCC recording setup.

Fig. 2. Time dependences of voltage at CdS sample and circuit current: general view (a), section A in enlarged time scale (b).

recorded in the waw format at the sampling frequency 96 kHz using a suitable software. The signal was processed using two channels simultaneously. This makes it possible to trace the switching dynamics in time and to evaluate the switching rate. The voltage amplitude value was controlled using a multimeter. The CdS film surface areas corresponding to junctions with point contacts were examined using a raster electron microscope.

The switching periods from HR to LR state and vice versa are of considerable interest to understand the physical and structure nature of the switching phenomena. To determine these parameters, the measuring device was used (Fig. 1) allowing us to record simultaneously the AC voltage changes at the sample and the circuit current using the voltage drop across the ballast resistor. As to the switching period evaluation, there is a limitation associated with the sampling frequency of the signal to be recorded that is 96 kHz in our case. Thus, the lower limit of the time record is 10.4 μs.

Let some voltage U_{sp} and current I time-based sweeps be considered that are typical of the samples under study. The AC voltage at the sample was varied in step-by-step fashion with an exposure of 2 to 3 s after each voltage increment. As the threshold voltage U_{th} is attained, a jump-like voltage drop and circuit current increase take place (Fig. 2). The transition to the stable LR state itself occurs during 3 or 4 AC voltage periods. The sample resistance in the HR state is about $5 \cdot 10^6$ Ω while in the LR one, about 500 Ω, that is, the LR to HR current ratio amounts 10^4. The calculated differential resistance R_d is about 1600 Ω. Effect of the applied voltage polarity on the samples at different voltage amplitude was studied. The switching effects have been found to take place also at the voltage sign change.
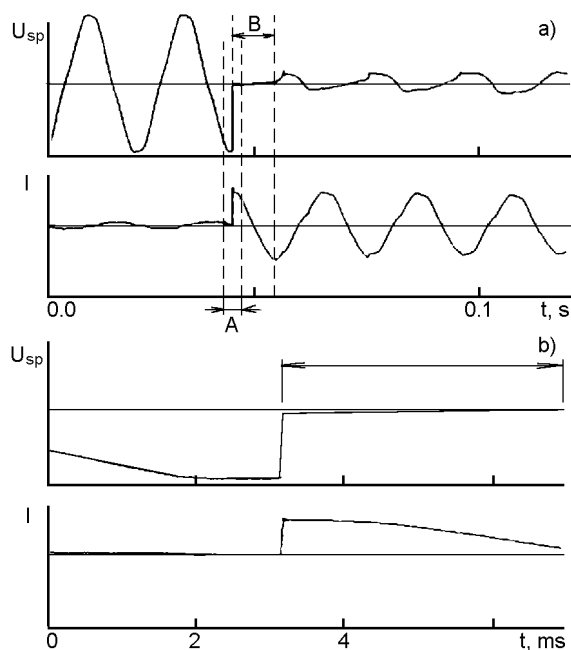
Besides, the effect of the pin pressed electrode material on the switching parameters was also a problem under consideration. To that end, the molybdenum pressed electrode was changed by the palladium one. This change, however, did not effect the registered switching patterns.

In Fig. 2b, the A section of the switching diagram presented in Fig. 2a is shown at the maximum possible expansion of the time scale. From the Figure, the HR to LR switching period t_{sw} can be estimated as 41.6 μs. In this expanded scale, the damping oscillations preceding the stable U_{sp} and I sections are clear to see. In Fig. 2a, a time interval following the switching moment is seen where the current channel works in the voltage stabilization mode at varying current (the B section). Fig. 3a presents a diagram similar qualitatively to that of Fig. 2. Here, of interest is the LR to HR switching period that is shorter than 10.4 μs. In Fig. 3b, a single-threshold HR to LR switching followed by the spontaneous re-switching to HR. It follows from consideration of numerous diagrams that the spontaneous switching effects may also be multiple. The next diagram (Fig. 3c) is also of a considerable interest. The sample is switched from the HR to LR_1 state that is unstable, since U_{sp} amplitude variations are seen. Further, this intermediate LR_1 state is switched spontaneously into a lower-resistance LR_2 one.
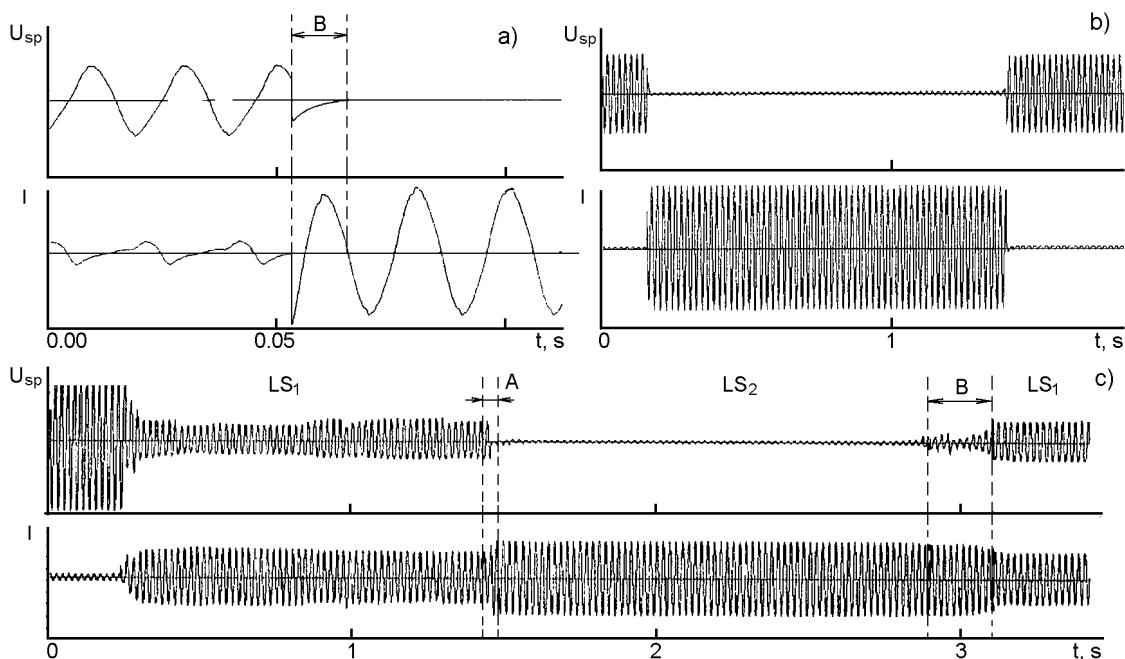
Fig. 3. U_{sp} and I time dependences with the asynchronous section (a), with spontaneous switching (b), and with two-stage switching to LR state (c).

Thus, a two-stage switching occurs. The LR_1 to LR_2 switching period can be evaluated to be shorter than 20.8 μs. The LR_2 state is maintained for some time but the opposite LR_2 to LR_1 switching takes place after an oscillation period. The electron microscopy has shown that the contact areas of the pin electrode with the film surface after the switching look as those with different extent of electron emission. This evidences an increased structure inhomogeneity due to the switching in the near-surface film area contacting immediately with the pin contact.

The work results are in our opinion of a considerable importance for the understanding of the switching phenomena nature. To explain the switching and memory effects, let the crystal-chemical features of CdS compound be considered. A high equilibrium vapor pressure of Cd as compared to S results in that the condensation from the vapor flow occurs at a Cd excess. Moreover, the considerable inconsistency between the liquidus and solidus lines in the phase diagram of the Cd–S system [9] results in a significant segregation of Cd and CdS components during the crystallization. The traditional model of CdS_{1-x} non-stoichiometric compound supposes the presence of point defects homogeneously distributed in the crystal bulk as interstitial cadmium atoms and sulfur vacancies. Such defects influence significantly the conductivity of the non-
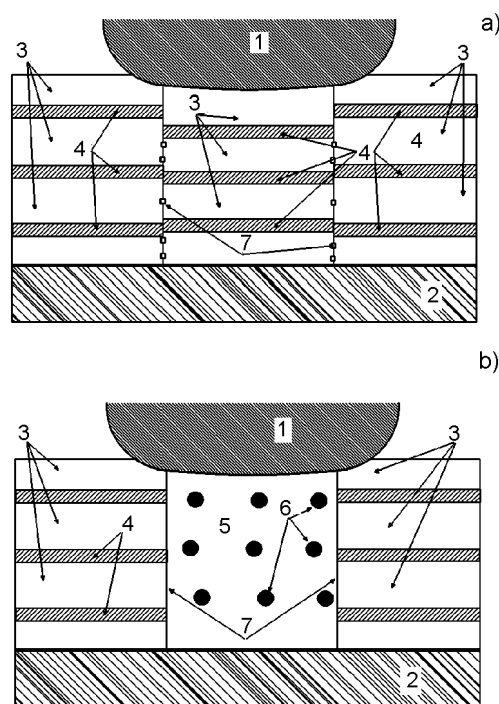

Fig. 4. Structure model of CdS film in the HR (a) and LR (b) states: point contact (*1*), counterelectrode (*2*), CdS layers (*3*), Cd layers (*4*), CdS_{1-x} region (*5*), point defects (*6*), grain boundaries (*7*).

stoichiometric compound. A new non-stoichiometric compound model distinct from the commonly adopted one is proposed

to explain the switching effects. The model is presented in Fig. 4.

According to the CdS–S system phase diagram [9], the non-stoichiometric compound crystallization occurs as follows. As the temperature decreases lower than the liquidus line, CdS grains start to crystallize. The excess Cd is driven away by the crystallization front, being remaining in the liquid phase. This driving-away of Cd lasts until its amount becomes a serious obstacle for the further growth of CdS crystal. This factor hindering the free energy decrease of the system being under cooling is eliminated due to the Le Chatelier principle. That is, the accumulated Cd atoms are crystallized in epitaxial fashion on the close-packed (0001) plane of CdS and form one or more pure Cd layers. This is followed by the further CdS growth. As the next CdS layer attains a certain thickness, the Cd interlayer is formed again. Thus, the stacks of crystallographic planes consisting of the excess component atoms grow at the interlayer boundaries between the stoichiometric CdS grains. Note that such a modulated "two-phase" structure, according to the phase diagram [9], answers to two-phase equilibrium for materials having a composition shifted to left from the stoichiometric one on the concentration axis of the diagram.

Initially, such a sample is in the high-resistance (HR) state (Fig. 4a). A ballast resistor $R_n = R_{n1}$ is switched in series with the sample. The voltage U_c applied to the circuit is distributed between the sample resistance R_{sp} and R_{n1}. The film is supposed to be somewhat locally heterogeneity, for example, over its thickness. If the electric power $W_{el} = I \times U$ applied to such an active region exceeds the scattered power ($W_{el} > W_{sc}$), that is, a certain threshold voltage is attained, a local temperature increase occurs in the active region. Such temperature increase, according to the phase diagram (Fig. 5), results in a reaction between the liquid Cd phase and solid CdS one: $Cd_L + CdS_S \rightarrow (CdS_{1-x})_L$. At the further temperature increase, the amount of the stoichiometric solid CdS phase will decrease while that of the non-stoichiometric liquid CdS_{1-x} one, increase. The liquid phase composition will vary according to the left conode end along the liquidus line as the conode moves up along the temperature axis. Thus, as the temperature increases from the solidus point up to the liquidus one, the diffusion-induced homogenization
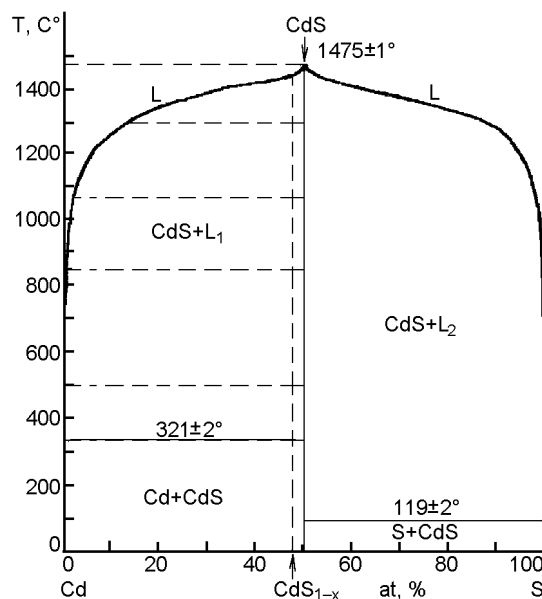

Fig. 5. Phase diagram of Cd–S system.

of the system occurs from the Cd + CdS composition to the CdS_{1-x} one. In accordance to that structure variation, the active region, that is, the material in a local region of the interelectrode space, is transformed from the HR state of CdS into the LR one of CdS_{1-x}. The structure homogenization process and the accompanying resistivity change of the active region is propagated over the whole film thickness. The initial HR state of the active region is changed to the LR one (Fig. 4b). The LR stabilization occurs due to decrease of the voltage drop on the active region of the film caused by a dramatic increase of its proportion on the ballast resistor. The active region is cooled instantly and the heterogeneous non-stoichiometric CdS_{1-x} state becomes "frozen" therein.

The reverse LR-to-HR switching occurs in another thermal regime set by selection of another R_n value $R_{n2} < R_{n1}$. While at the forward switching (HR→LR) the resistivity ρ of the active region was changed by a factor of 10^4 due to its homogenization, now, under the homogeneous LR state heating and melting, the ρ change amounts is as small as several tens per cent only. In this case, the voltage drop redistribution between the CdS film active region and the ballast resistor results in such a relation between the heat release W_{el} and heat scattering W_{sc} that a rather slow cooling of the current channel takes place instead of its quenching. In this case, a quasi-equilibrium two-phase crystallization occurs. According

to the phase diagram, the CdS phase is crystallized first, that is, the HR phase fills the current channel. The liquid phase of decreasing volume will get rich in cadmium according to displacement of the left conode end towards the solidus line. As a result, the Cd interlayers between stoichiometric CdS blocks will be restored, thus, the HR state will be formed (Fig. 4a).

Basing on the proposed structure model of the switching and memory, the features of the process dynamics observed in our experiments are easy to explain. The spontaneous reversible switching (Fig. 3c) can be observed repeatedly if the ballast resistor is selected so that the loading line coincides with the S-shaped NDR section of the VCC [10]. In this case, the HR→LR transformation is accompanied by the voltage increase at R_n. The electric power applied to the current channel becomes decreased as compared to the scattered one, so that the channel slow cooling mode occurs, thus, the transition to HR, that is, to the initial state. In that fashion, cyclic phase transitions in the active region and periodic oscillations of the circuit current are realized. In diagrams presented in Figs. 2 and 3a, there is an unusual section B evidencing the so-called latent switching period. The establishing of stable conductivity characteristics in both HR and LR states is seen to be not an instantaneous process. Thus, the system exhibits a certain inertia in that it responses to the electric regime changes with some delay. In our opinion, this fact evidences that the switching and memory effects are based not on electron re-buildings but on atomic structure ones. The section B in Figs. 2 and 3a demonstrates a distorted synchronicity in the $U(t)$ and $I(t)$ changes in the active zone. In our opinion, this time interval, when being recorded and measured, makes it possible to obtain some new physical data on the switching process. The synchronicity violation between U and I changes in the active region is due to that thermal processes show a time lag as compared to the used alternating voltage period. The structure changes in the active region do not trace the alternating voltage phase changes but the thermal effect dynamics. So, for example, it is seen in Fig. 3a that the switching took place in a moment $U < U_{amp}$. Thus, the duration of the HR→LR transitions answers to the time lag between $I(t)$ and $U(t)$. In timebase deflections of $U_{sp}(t)$ and $I(t)$ (Fig. 3), a double-threshold HR→LR$_1$→LR$_2$ switching is ob-

served. It can be explained also using the model proposed. At certain distance ratios between the non-uniformly distributed excess cadmium interlayers, a situation becomes possible when the transition into LR due to the applied electric power takes place only in a part of the film thickness. In this case, the total resistance of the region decreases somewhat, that is, an intermediate LR$_1$ state arises. As W_{el} increases, the LR may become propagated through the whole CdS film thickness, thus, the LR$_2$ occurs.

To conclude, let some advantage of the novel structure model be pointed to. In some traditional models, the bistable switching is explained using concepts of electrodiffusion of the metal contact particles into the sample active region [11]. In this case, it is of importance to take into account the polarity of the applied rectified voltage. The refractoriness of the electrode material is also very important. Our experiments have shown that neither the electrode material changes nor the polarity changes of the rectified voltage result in substantial changes in the switching properties of the semiconductor films studied. These results are difficult to explain within the frame of the traditional switching and memory models. In contrast, in our model, both the electrode material changes and the applied voltage polarity changes should not influence the switching processes. Since there is an internal substance resource in the semiconductor layer, the diffusion transfer of metal particles out of the electrode, as supposed in [11], is unnecessary. A substantial advantage of the model proposed consists in a considerable shortening of the diffusion path during the current channel conductivity transformations as compared to the semiconductor metallization by the electrode [11]. As has been shown in our studied of the grain morphology in CdS films, at the grain size of 10 µm along the normal to the film surface, the average thickness of stacked plates is 20 to 30 nm.

Thus, a technique has been proposed and checked for recording dynamic parameter of the current instability phenomenon which made it possible to determine a set of kinetic and physical characteristics as well as new features of the switching phenomenon, including the transition process durations, the switching latency time, the possibility of intermediate conductivity states, the synchronicity violation between the changes of voltage at the sample and circuit current, the independence of the switching charac-

teristics of the electrode material and the voltage polarity, and the possibility of spontaneous reversible multiple switching. A novel structure model has been proposed for the switching and memory in CdS films that makes it possible to explain a large number of experimental facts basing on the common concept, in contrast to the traditional model of that phenomenon.

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Структурна модель бістабільного перемикання струму у плівках CdS

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Отримано ВАХ плівок CdS у статичному та динамічному режимах. Виявлено ряд нових особливостей кінетики електростимульованого перемикання між двома стабільними станами, які відрізняються за рівнем електропровідності в 10^4 разів і зберігаються після відключення зовнішньої напруги. Запропоновано нову структурну модель бістабільного перемикання.