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An analytical accumulation mode SOI pMOSFET model for high-temperature analog applications

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Abstract. An accumulation mode SOI pMOSFET model for simulation of analog circuits meant for high-temperature applications is presented in the paper. The model is based on explicit expressions for the drain current with an infinite order of continuity what assures smooth transitions between different operation regimes of the transistor. This model is valid for all regimes of normal operation, demonstrates proper description of high-temperature behavior of the subthreshold and off-state current. The model characteristics show a good agreement with the experimental data for temperatures up to 300 °C.

Keywords: high-temperature electronics, AM SOI pMOSFET, C_{∞} -continuous model.

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1. Introduction

Nowadays high-temperature electronics is a very important technology, especially for oil & gas, aerospace and automotive industries. Micronic silicon-on-insulator (SOI) CMOS technologies have proved to be the most mature for the 200-350 °C range of operation [1]. In particular, accumulation-mode (AM) SOI pMOSFETs appear very promising for the design of analog circuits operating in the wide temperature range (up to 350 °C)[1]. For developing these circuits, it is necessary to have an AM SOI pMOSFET model that is continuous in all regimes of operation, and derivatives of which are also continuous (C_{∞} -continuous model). Such model has not been developed yet for high temperatures. In this paper, we present an extension to high temperatures of the room-temperature models developed by B. Iñiguez *et al.* [2, 3].

2. Model

As it is well known, the AM SOI MOSFETs feature three possible conduction modes: conduction through front and back accumulation layers (accumulation channels) and that through the non-depleted portion of

the Si film, *i.e.*, the quasi-neutral region (body channel) [4, 5]. The AM SOI pMOSFET model [2] accounts only two of these conduction modes, which are important under typical circuit operation (see Fig. 1b): body current and accumulation current, which appears when a portion of the front surface is in accumulation. *I.e.*, the model is valid under the conditions, first, that the back surface of the Si film is always depleted, there are no mobile charge at the back interface and therefore current does not flow at the back interface; and second, the body current always appears in a central quasi-neutral region of the film before front accumulation develops (*i.e.*, when the gate voltage is swept to negative values in a pMOSFET).

However, there also exists a special case of full depletion of the AM SOI pMOSFET film by back-gate bias and positive charge in the buried oxide (BOX), which appears if the doping of Si film is low. This special case can be handled using the equations similar to the fully depleted (FD) SOI nMOSFET model [3]. This is justified because in both cases the Si film is fully-depleted, and the conduction takes place in the (accumulation or inversion) channel at the front Si/SiO₂ interface [6].

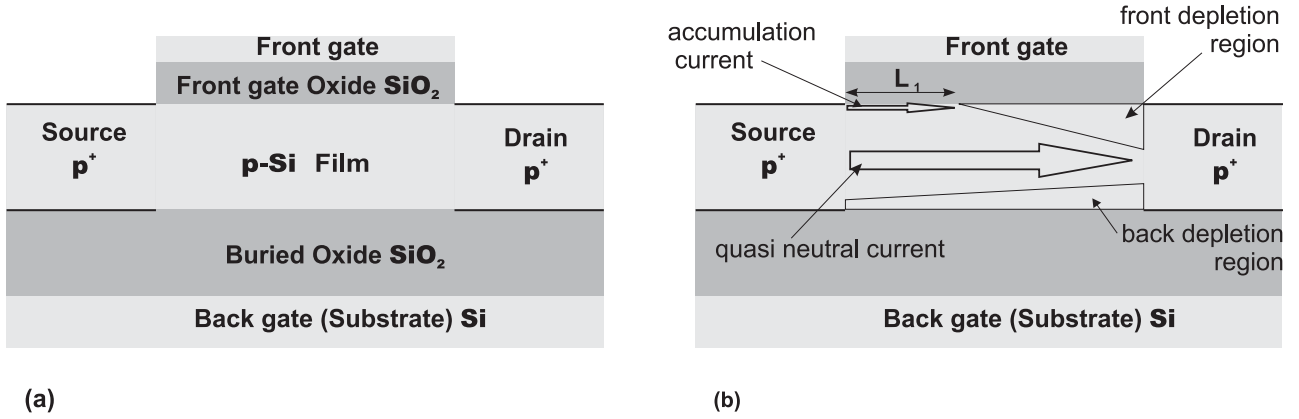


Fig. 1. Cross section of an AM SOI pMOSFET (a) and conduction in an AM SOI pMOSFET with the front surface partially depleted, partially accumulated (b).

Therefore, for the first time we develop a high-temperature model for AM SOI pMOSFETs based on the room-temperature models for AM SOI pMOSFETs [2] and FD enhancement mode (EM) nMOSFETs [3].

2.1. Overview of room-temperature AM SOI pMOSFET model with body channel

A. Front surface depleted

The width of the body current path depends on the depth of the depletion regions controlled by the front and the back gates. The back depletion depth, x_{db} , can be assumed to be constant along the channel [4, 7] and equal to

$$x_{db} = -\frac{\varepsilon_{Si}}{c_{ob}} + \sqrt{\left(\frac{\varepsilon_{Si}}{c_{ob}}\right)^2 + 2\varepsilon_{Si} \frac{V_{gb} - V_{fbb}}{qN_a}}. \quad (1)$$

The front depletion depth at a certain point of the channel can be written as

$$x_{df} = -\frac{\varepsilon_{Si}}{c_{of}} + \sqrt{\left(\frac{\varepsilon_{Si}}{c_{of}}\right)^2 + 2\varepsilon_{Si} \frac{V_{gf} - V_{fbf} - V_c}{qN_a}}. \quad (2)$$

In (1) and (2), c_{of} and c_{ob} are the front and back oxide capacitances, ε_{Si} and N_a are dielectric permittivity and doping level, respectively, V_{gf} and V_{gb} are the front and back gate voltages, respectively, and V_c is the channel voltage in a given point of the channel. V_{fbf} and V_{fbb} are the front and back flat-band voltages. We define the effective film thickness as $t_{b,eff} = t_b - x_{db}$, where t_b is the silicon film thickness. Therefore, the body channel thickness at each channel point is $x_{ch} = t_{b,eff} - x_{df}$. The mobile charge density in the body channel is obtained as $q_{bc} = qN_a x_{ch}$. The

threshold voltage V_{thf} is defined at the minimum front gate voltage that pinches off the channel at $V_c = 0$, that is [7]

$$V_{thf} = V_{fbf} + \frac{t_{b,eff} q N_a}{c_{of}} + \frac{t_{b,eff}^2 q N_a}{2\varepsilon_{Si}}.$$

However, even when the whole silicon film is fully depleted below the threshold, there is still a diffusion current component (the subthreshold component) that depends exponentially on $V_{gf} - V_{thf}$ [8].

To develop a unified model, we have to consider both the drift (that dominates above the threshold) and the diffusion term (that dominates below threshold) of the body current. We define the effective potential ψ in order to extend (2) below the threshold, so that the resulting q_{bc} is written as

$$q_{bc} = qN_a \left[t_{bt} - \sqrt{\left(\frac{V_{gft} - \psi}{qN_a} 2\varepsilon_{Si}\right) + t_{bt}^2} \right], \quad (3)$$

where $t_{bt} = t_{b,eff} + \varepsilon_{Si}/c_{of}$, and $V_{gft} = V_{gf} - V_{thf}$.

Hence, (3) is a generalization of (2) in which we have replaced V_c by the effective potential ψ in order to extend the validity of the expression of q_{bc} into the subthreshold regime. In the subthreshold regime, q_{bc} depends exponentially on $V_{gf} - V_{thf}$ [8]. So, ψ tends to V_c above the threshold, and in the subthreshold it tends to a value that gives such dependence of q_{bc} .

Therefore, the relationship between ψ and q_{bc} is

$$d\psi = -\frac{1}{\varepsilon_{Si}} \left(\frac{q_{bc}}{qN_a} - t_{bt} \right) dq_{bc}. \quad (4)$$

We write the body channel current as the sum of the drift and diffusion terms

$$I_{bcd} = -W\mu_b \left(q_{bc} \frac{d\psi}{dx} - v_T \frac{dq_{bc}}{dx} \right), \quad (5)$$

where μ_b is the mobility in the silicon film, and $v_T = kT/q$ is the thermal voltage.

Using (3) in (4), we obtain the following expression of the body channel current when the front surface is fully depleted:

$$I_{bcd} = \frac{W}{L} \mu_b \left[\frac{1}{3qN_a \varepsilon_{Si}} (q_{bc,d}^3 - q_{bc,s}^3) - \frac{t_{bt}}{2\varepsilon_{Si}} (q_{bc,d}^2 - q_{bc,s}^2) - v_T (q_{bc,d} - q_{bc,s}) \right], \quad (6)$$

where $q_{bc,s}$ and $q_{bc,d}$ are the body channel mobile charge densities at the source and drain ends, respectively.

B. Front surface accumulated

When a portion of the front surface is in accumulation, the accumulation charge density at a point of the surface can be written as [7]

$$q_{ac} = -c_{of} (V_{gf} - V_{jbf} - V_c). \quad (7)$$

Writing the accumulation current as $I_{ac} = W\mu_{ac}(-q_{ac})dV_c/dx$ (μ_{ac} being the surface mobility) and using from (7) $dV_c = dq_{ac}/c_{of}$ we get assuming the front surface is accumulated from source to drain

$$I_{ac} = \frac{W}{L} \mu_{ac} \left[\frac{1}{2c_{of}} (q_{ac,s}^2 - q_{ac,d}^2) \right], \quad (8)$$

where $q_{ac,d}$ and $q_{ac,s}$ are the accumulation charge densities at the source and drain ends, respectively, obtained from (7).

When the front surface is fully accumulated, neglecting the thickness of the accumulation layer, the body current is written as

$$I_{bcnd} = -\frac{W}{L} \mu_b q N_a t_{b,eff} V_{ds} = \frac{W}{L} \mu_b \frac{N_a q t_{b,eff}}{c_{of}} (q_{ac,d} - q_{ac,s}), \quad (9)$$

where 'bcnd' index stands for 'Body Current at Non-Depleted front surface', and V_{ds} is the drain-source voltage.

C. Front surface partly accumulated, partly depleted

To develop a unified model, we have to assume that there can be a portion of the channel with accumulation

at the surface (from the source, $x=0$, to a length $x=L_1$, see Fig. 1b) and a portion with depletion at the surface (from $x=L_1$ to the drain, $x=L$). By integrating the drift-diffusion equation from source to drain, we obtain

$$\int_0^L I_{ds} dx = W \int_0^{L_1} (-\mu_{ac} q_{ac} - \mu_b q N_a t_{b,eff}) dV_c + W \int_{L_1}^L \mu_b (v_T dq_{bc} - q_{bc} d\psi). \quad (10)$$

To integrate, we make the following variable changes: between $x=0$ and $x=L_1$ we can write $dV_c = dq_{ac}/c_{of}$ from (7). Between $x=L_1$ and $x=L$, we can write $d\psi = -1/\varepsilon_{Si} (q N_a - t_{bt}) dq_{bc}$ from (4). To obtain an analytical solution, we assume that the effective mobilities μ_b and μ_{ac} are independent of the position on the channel (as we will discuss below, μ_{ac} depends on the applied voltages).

We get

$$I_d = \frac{W}{L} \mu_{ac} \left[\frac{1}{2c_{of}} (q_{ac,s}^2 - q_{ac,p}^2) \right] + \frac{W}{L} \mu_b \frac{N_a q t_{b,eff}}{c_{of}} (q_{ac,p} - q_{ac,s}) + \frac{W}{L} \mu_b \left[\frac{1}{3qN_a \varepsilon_{Si}} (q_{bc,d}^3 - q_{bc,p}^3) - \frac{t_{bt}}{2\varepsilon_{Si}} (q_{bc,d}^2 - q_{bc,p}^2) - v_T (q_{bc,d} - q_{bc,p}) \right] \quad (11)$$

where $q_{bc,p}$ and $q_{ac,p}$ are the quasi-neutral and accumulation charge densities at $x=L_1$, respectively. Therefore, $q_{ac,p}=0$ and $q_{bc,p} = q N_a t_{b,eff}$.

Eq. (11) can be extended to all the possible regimes (including the surface accumulated from the source to drain and that depleted from the source to drain) replacing $q_{ac,p}$ by $q_{ac,d}$ and $q_{bc,p}$ by $q_{bc,s}$:

$$I_d = \frac{W}{L} \mu_{ac} \left[\frac{1}{2c_{of}} (q_{ac,s}^2 - q_{ac,d}^2) \right] + \frac{W}{L} \mu_b \frac{N_a q t_{b,eff}}{c_{of}} (q_{ac,d} - q_{ac,s}) + \frac{W}{L} \mu_b \left[\frac{1}{3qN_a \varepsilon_{Si}} (q_{bc,d}^3 - q_{bc,s}^3) - \frac{t_{bt}}{2\varepsilon_{Si}} (q_{bc,d}^2 - q_{bc,s}^2) - v_T (q_{bc,d} - q_{bc,s}) \right]. \quad (11')$$

When the front surface is accumulated from the source to $x = L_1$, $q_{acd} = 0$ and $q_{bc,s} = qN_a t_{b,eff}$, and therefore, (11') gives (11). When the front surface is accumulated from source to drain, $q_{bc,s} = q_{bc,d} = qN_a t_{b,eff}$, and (11') reduces to $I_{ds} = I_{ac} + I_{bcd}$ as it should. When the front surface is depleted from the source to drain $q_{ac,s} = q_{acd} = 0$, and (11') reduces to $I_{ds} = I_{bcd}$ as it should, too.

Therefore, we can write $I_{ds} = I_{ac} + I_{bcd} + I_{bcd}$ provided I_{ac} , I_{bcd} and I_{bcd} are written as (6), (8) and (9), respectively. Please, note that this does not mean that the total channel current is considered as the sum of three components in parallel; in fact these two components of the body current appear in series, but they are not written as (6) nor (9), because one component flows in a length equal to L_1 and the other one flows in that equal to $L - L_1$.

D. Continuous expressions

To further develop the unified single-piece model, we need to approximate unified expressions for accumulation and quasi-neutral (body) charges at source and drain ends $q_{ac,s}$, q_{acd} , $q_{bc,s}$, and $q_{bc,d}$, respectively, valid from the subthreshold to total accumulation regime. We introduced the effective potential ψ in (3) for that. As an explicit expression, we use a suitable interpolation function V_{gfte} instead of $V_{gfti} = V_{gft} - \psi$. Above the threshold, when $V_{gf} = V_{fbf} + V_c$, this interpolation function should smoothly give $q_{bc} = qN_a t_{b,eff}$. So, we have the following expression for the quasi-neutral mobile charge density:

$$q_{bc} = qN_a \left[t_{bt} - \sqrt{\left(\frac{V_{gfte}}{qN_a} 2\varepsilon_{Si} \right) + t_{bt}^2} \right] \quad (12)$$

and

$$V_{gfte} = V_{pe} \left[1 - \frac{\log(1 + \exp[A_{PS}(1 - V_{gfte0}/V_{pe})])}{\log(1 + \exp[A_{PS}])} \right], \quad (13)$$

where $V_{pe} = V_{fbf} - V_{thf}$, A_{PS} in (3) is a fitting parameter that controls the transition from depletion to diffusion of the depleted charge in an AM SOI pMOSFET, it makes $\exp(A_{PS}) \gg 1$, and V_{gfte0} is the following interpolation function:

$$V_{gfte0} = nv_T - \sqrt{(nv_T)^2 + 4V_{gfte00}^2}, \quad (14)$$

where

$$V_{gfte00} = -nv_T S_{NT} \log \left(1 + \exp \left[\sqrt{\frac{v_0}{nv_T S_{NT}^2} - \frac{(V_{gft} - V_c)}{2nv_T}} \right] + \exp \left[\frac{-(V_{gft} - V_c)}{2nv_T S_{NT}} \right] \right). \quad (15)$$

S_{NT} (< 1) is the parameter that controls the transition from below to above threshold, v_0 is a fitting parameter that controls the magnitude of the body charge density above the threshold, and n corresponds to the subthreshold slope.

Above the threshold and below the flat band ($V_{fbf} + V_c < V_{gf} < V_{thf} + V_c$), $V_{gfte0} > V_{pe}$ and $V_{gfte} \cong V_{gfte0} \cong V_{gft} - V_c$, as it should; below threshold, still $V_{gfte} > V_{pe}$ and $V_{gfte} \cong V_{gfte0}$, but from (14) and (15) we get that to the first order V_{gfte0} is proportional to

$$\exp \left(-\frac{V_{gft} - V_c}{nv_T} \right);$$

substituting (14) in (13) we obtain

$$\text{from (12) that } q_{bc} \text{ is, to the first order, proportional to } \exp \left(-\frac{V_{gft} - V_c}{nv_T} \right),$$

as it should. Above the flat band $V_{gfte0} < V_{pe}$ (note that for SOI pMOSFET V_{gfte0} and V_{pe} are both negative) and hence $V_{gfte} \cong V_{pe}$ and $q_{bc} \cong qN_a t_{b,eff}$, as it should.

In the expression for I_{bcd} (6), we calculate $q_{bc,s}$ and $q_{bc,d}$ from Eqs (12)-(15) for V_c equal to the source voltage V_s and to the drain voltage V_d , respectively, therefore I_{bcd} tends smoothly to the desired limits in the different regimes.

The diffusion term – the latter term in Eq. (6) – only dominates in the subthreshold regime. Due to intrinsic overestimation in the calculation of q_{bc} by using Eq. (12), which can affect the near-threshold regime, we modify (6) by using, instead of v_T , the factor

$$v_{T0} = \frac{v_T}{1 - (V_{gfte0,s}/v_T + V_{gfte0,d}/v_T)},$$

where $V_{gfte0,s}$ and $V_{gfte0,d}$ are calculated from Eq. (14) at $V_c = V_s$ and $V_c = V_d$, respectively. Therefore, $v_{T0} \cong v_T$ in the subthreshold, as it should, and it tends to zero above the threshold. This modification improves the accuracy near the threshold.

For the accumulation charge density, we present a useful unified expression that does not require interpolation functions more than those used to calculate $q_{bc,s}$ and $q_{bc,d}$

$$q_{ac} = -c_{of}(V_{gfe0} - V_{gfe}). \quad (16)$$

It is clear that (16) tends to the desired limits in all regimes. Below the flat band $V_{gfe} \cong V_{gfe0}$ and $q_{ac} = 0$. Above the flat band $V_{gfe} = V_{pe}$ and $V_{gfe0} = V_{gft} - V_{thf} - V_c$ and, hence, $q_{ac} = -c_{of}(V_{gf} - V_{fbf} - V_c)$, as it should.

Calculating q_{acs} and q_{acd} from (16) with $V_c = V_s$ and $V_c = V_d$, we get an explicit C_∞ -continuous model for I_{ac} and I_{bcnd} . Therefore, $I_{ds} = I_{ac} + I_{bcnd} + I_{bcd}$ is the expression of the total channel current in all regimes.

2.2. Second-order effects

Here we improve the model by including the second-order effects such as vertical and lateral field effects, channel-length modulation and series resistance [2]. Generally, influence of such effects is not very important at the used channel length, but it could be noticeable at large drain voltages (in the saturation regime), and become much more significant with decreasing the channel length. In this subsection, we describe briefly the main second-order corrections used in the model [2].

A. Vertical field effect

In the above analysis, we have not considered the degradation of the surface mobility along the channel. However, we can keep the same equations using an effective surface mobility $\mu_{ac,eff}$ which accounts for mobility degradation with the average normal field in the accumulation channel. A useful expression for mobility degradation is

$$\mu_{ac,eff} = \frac{\mu_{ac}}{1 + \alpha \langle E_{sf} \rangle}, \quad (17)$$

where $\langle E_{sf} \rangle = (q_{ac,s} + q_{ac,d})/2\epsilon_{Si}$ is the average field along the channel of the normal in the accumulation layer.

There is no degradation of the body mobility μ_b , since the normal field is low in the body region.

B. Lateral field effect

However, both the body and surface components of the current are affected by the velocity saturation effect. We assume that the drift velocity of charge carriers in the body can be written as $v = \mu_b(d\psi/dx)/(1 - \mu_b/[2v_{sat}]d\psi/dx)$ if $d\psi/dx < 2v_{sat}/\mu_b$ and as $v = v_{sat}$ if $d\psi/dx > 2v_{sat}/\mu_b$, where v_{sat} is the saturation velocity.

Following the same procedure as in Section 2.1, but integrating the drift-diffusion equation from $x=0$ to $x=L_{eff}$ (L_{eff} being the effective length where the gradual channel approximation is valid, i.e., $d\psi/dx < 2v_{sat}/\mu_b$; we will define this length later), we finally get the same expression of the body current $I_{bcd} + I_{bcnd}$ as in the Section 2.1, but with μ_b replaced by $\mu_b/(1 - V_{dse}/V_{L,b})$, where $V_{L,b} = 2v_{sat}L_{eff}/\mu_b$, and V_{dse} is the effective drain-source voltage. Assuming the same velocity-field relationship for the surface component, I_{ac} has the same expression as in Section 2.1, but with μ_{ac} replaced by $\mu_{ac,eff}/(1 - V_{dse}/V_{L,ac})$, where $V_{L,ac} = 2v_{sat}L_{eff}/\mu_{ac,eff}$.

V_{dse} is defined as an interpolation function that tends to V_{ds} in the linear regime and to saturation voltage V_{dsat} in the saturation one:

$$V_{dse} = V_{dsat} \left[1 - \frac{\log(1 + \exp[A_{TS}(1 - V_{ds}/V_{dsat})])}{\log(1 + \exp[A_{TS}])} \right], \quad (18)$$

where A_{TS} is a fitting parameter that controls the transition from the linear regime to saturation. In the subthreshold, the effect of saturation velocity is negligible and V_{dse} should tend to zero.

The saturation voltage is defined as the drain-source voltage, at which in the quasi-neutral region the carriers travel at a constant velocity, the saturation velocity v_{sat} . It is obtained by equating the expression of I_{ds} to $I_{ds} = Wv_{sat}qN_a t_{b,eff}$. In our case, it cannot be found analytically, so we use a special approximation again, valid in all operation regimes owing to the use of the interpolation function (14)

$$V_{dsat} = V_{gfe0,s} - \frac{V_{gfe0,s}}{V_{gfe0,s} - v_T} \frac{I_{ds}|_{V_{dse}=V_{gfe0,s}}}{Wv_{sat} \epsilon_{Si} / t_{bt}}, \quad (19)$$

where $I_{ds}|_{V_{dse}=V_{gfe0,s}}$ is the unified expression of the drain current at $V_{dse} = V_{gfe0,s}$ (that is, when $q_{bc,d}$ and $q_{ac,d}$ are negligible). V_{dsat} tends to $V_{gfe0,s}$ in the subthreshold, which allows to get the desired expression of $q_{bc,d}$, and above the threshold it tends to the desired saturation voltage.

C. Channel length modulation

When the body conduction is in the saturation regime, the channel length modulation effect has to be accounted for. We write $L_{eff} = L - l_{sat}$, where l_{sat} is the modulated channel length:

$$l_{\text{sat}} = l_d \log \left(\frac{c_1 + \sqrt{c_1^2 + c_2^2}}{c_2} \right), \quad (20)$$

where $c_1 = V_{ds} - V_{dse}$, $c_2 = l_d v_{\text{sat}} / \mu_b$, and l_d is the characteristic length that is considered as adjustable parameter.

D. Series resistance

The effect of the series drain and source resistance is included to the first order by a multiplication factor:

$$I_d = f_R I_{d,i}, \quad (21)$$

where $I_{d,i}$ is the drain current expression without accounting for the series resistance and $f_R = 1/(1 + a_{R1} + a_{R2})$, where

$$a_{R1} = \mu_{ac,\text{eff}} c_{of} R_{\text{tot}} \frac{W}{L} \left(\frac{q_{ac,s} + q_{ac,d}}{2c_{of}} \right), \quad (22)$$

$$a_{R2} = \mu_b \frac{R_{\text{tot}}}{2} \frac{W}{L} (q_{bc,s} + q_{bc,d}), \quad (23)$$

and R_{tot} is the total parasitic drain-source resistance.

2.3. Fully-depleted AM SOI pMOSFET room-temperature model

Here we consider the case of fully-depleted low-doped AM SOI pMOSFET, deriving it from the FD EM SOI nMOSFET model [3].

A. Overview of FD EM SOI nMOSFET room-temperature model

The C_∞ -continuous FD enhancement mode (EM) SOI nMOSFET model [3] is based on the physical expression for the mobile charge density in the front inversion channel Q_{nf} :

$$Q_{nf} = c_{of} n_S v_T \left[1 - \sqrt{1 + \frac{4Q_{nf2}^2}{(c_{of} n_S v_T)^2}} \right], \quad (24)$$

where n_S is the subthreshold slope ideality factor, and Q_{nf2} is a special approximation function:

$$Q_{nf2} = -c_{of} n_S v_T S_{NT} \times \log \left[1 + \frac{1}{4S_{NT}} \exp \left(\frac{V_{Gf} - V_{\text{thf},i} - n_S V_c}{2n_S v_T} \right) + \exp \left(\frac{V_{Gf} - V_{\text{thf}} - n_S V_c}{2n_S v_T S_{NT}} \right) \right]. \quad (25)$$

In (25) the second term in the logarithm dominates in weak inversion and the third one in strong inversion. Here n stands for the body factor in strong inversion. S_{NT} controls the transition from weak to strong inversion ($S_{NT} < 1$). $V_{\text{thf},i}$ being the front threshold voltage which corresponds to a surface potential of $2\phi_F + V_c$ (ϕ_F is the Fermi potential). While this threshold value appears in a weak inversion term of (25), a different value is introduced in the strong inversion term, V_{thf} , to take into account that the strong inversion surface potential is always larger than $2\phi_F + V_c$ by a few v_T . This capability to use two threshold voltages is an advantage over other models, which have to artificially overestimate the mobility degradation, especially for moderate V_{gf} , in order to account for the threshold voltage increase from weak to strong inversion [9]. These two threshold voltages could be expressed as $V_{\text{thf},i} = V_{\text{thf}0,i} - (n-1)V_{gb}$ and $V_{\text{thf}} = V_{\text{thf}0} - (n-1)V_{gb}$, where $V_{\text{thf}0,i}$ and $V_{\text{thf}0}$ could be considered as fitting parameters or derived from other technology parameters.

The interpolation function (24) tends to the desired physically proper limits in weak and strong inversion and yields continuous expression for the current:

$$I_d = \mu_n \frac{W}{L} \left[v_T (Q_{nf,d} - Q_{nf,s}) - \frac{Q_{nf,d}^2 - Q_{nf,s}^2}{2nc_{of}} \right], \quad (26)$$

where μ_n is the electron mobility, $Q_{nf,s}$ and $Q_{nf,d}$ are the inversion charge densities at the source and drain edges, calculated from (26) for V_c equal to source voltage V_s and to drain voltage V_d , respectively.

B. Customization for the case of FD low-doped AM SOI pMOSFET

Therefore an explicit C_∞ -continuous model for FD EM nMOSFET is obtained in previous subsection. Here we demonstrate that it can be customized for the case of FD low-doped AM pMOSFET by appropriate change of voltage signs. Other device type dependent parameters, such as surface potentials, zero for weak accumulation and a few v_T lower for strong accumulation, are fully encapsulated in the two threshold voltages $V_{\text{thf},i}$ and $V_{\text{thf}0}$, which could be considered as fitting parameters again, or calculated from technological parameters of AM pMOSFET devices following [10]:

$$V_{\text{thf},i} = V_{fbf} + \frac{qN_a t_b}{2c_{of}} - \frac{c_{bb}}{c_{of}} \left(-V_{fbb} - \frac{qN_a t_b}{2c_{ob}} \right), \quad (27a)$$

$$V_{\text{thf}0} = V_{\text{thf},i} + n_S \phi_{sa}. \quad (27b)$$

Here c_{bb} is the capacitance of the film and the back oxide in series, $c_{bb} = c_b c_{ob} / (c_b + c_{ob})$, where $c_b = \epsilon_{Si} / t_b$ is the film capacitance, and ϕ_{sa} is the surface potential of strong accumulation. Now we can use $V_{thf,i}$ and V_{thf} in (25) with appropriate change of signs.

The second-order effects are introduced similarly as described in Section 2.2, for details please refer the original paper [3].

2.4. Developing of high-temperature model

A. General temperature dependences

Due to the fact that the C_∞ -continuous model described above was developed on physical principles and depends only on physical parameters of the device, there is clear possibility to introduce temperature dependences of all the parameters. Temperature dependences of all the main parameters of AM SOI pMOSFET (intrinsic carrier concentration n_i , bandgap width E_g , mobility μ , etc.) are well-known [11]. However, this is not enough to develop the high-temperature model, because some assumptions of the described above model are not valid at high temperatures.

B. Subthreshold slope at high temperatures

The main problem is that the potential distribution in the film at high temperatures differs significantly from the potential distribution at room temperature, and the charge-sheet model approximation which is used in the C_∞ -continuous models [2, 3] described in the previous sections becomes inaccurate [12]. As a result, we have considerable disagreement between the model and experimental curves in the subthreshold and off-state regions, while off-state currents at high temperatures becomes extremely large and can influence the normal operation of devices, so proper modeling of them is necessary. The models like [2, 3] described above predict linear behavior of the subthreshold slope dependence upon temperature, while our experiment states that this dependence is highly nonlinear. This was explained using numerical simulation by prevalence of diffusion component of current [12]. Instead of numerical simulations, we used an empirical dependence extracted from experimental data: a combination of 3rd power polynomial and exponential dependences (see Fig. 2):

$$S = C_1 e^{-T/300} + C_2 T^3 + C_3 T + C_4, \quad (28)$$

with the coefficients $C_1 = 2.41 \text{ V}^{-1}$, $C_2 = -4.07 \cdot 10^{-8} \text{ V}^{-1} \text{ K}^{-3}$, $C_3 = -0.01 \text{ V}^{-1} \text{ K}^{-1}$ and $C_4 = -2.23 \text{ V}^{-1}$.

C. High-temperature off-state currents

We consider two components of the off-state leakage currents in the accumulation mode p -channel device: current due to the thermal generation in the body film bulk (diffusion current) and current due to the thermal generation in the drain-depleted body film region (generation current).

The diffusion component is expressed as [11]

$$I_{osd} = \mu_b v_T \left(1 - e^{V_D/v_T}\right) \frac{q n_i^2}{N_a} t_b \frac{W}{L_c}, \quad (29)$$

where L_c is the diffusion length (or the effective device length if the latter is shorter). As it was showed previously [12], the total carrier density responsible for the diffusion component in the case of accumulation mode p -channel devices is the same as in the case of the enhancement mode n -channel ones, so we used common approximation for minority carrier density $\frac{q n_i^2}{N_a}$.

The generation current in the depleted region of the body near the drain is expressed as [11]

$$I_{osg} = \frac{q n_i}{\tau_g} W L_i t_b, \quad (30)$$

where

$$L_i = \sqrt{\frac{2 \epsilon_{Si} v_T}{N_a}} \left\{ \sqrt{\ln\left(\frac{N_a}{n_i}\right) - \frac{q V_D}{v_T}} - \sqrt{\ln\left(\frac{N_a}{n_i}\right)} \right\}, \quad (31)$$

L_i stands for the depth of depleted region near the drain, where the thermal generation rate is maximal and outside of it the rate is negligible, τ_g is the generation lifetime.

Therefore, the total off-state current is

$$I_{off} = I_{osd} + I_{osg}. \quad (32)$$

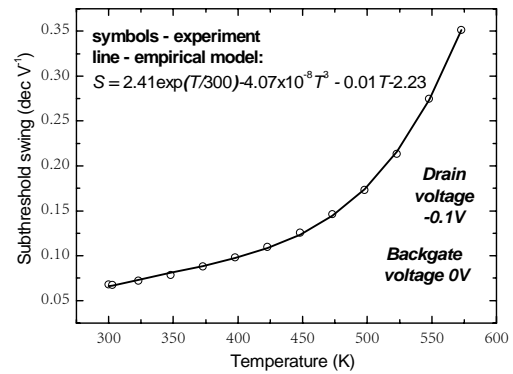


Fig. 2. Empirical dependence of the subthreshold slope upon temperature derived from experimental data.

3. Results and discussion

3.1. Fully-depleted AM SOI pMOSFET room-temperature model

The obtained model was validated using experimental data, obtained for AM SOI pMOSFET devices, fabricated on UNIBOND material in DICE, UCL (Belgium). The devices possessed the following parameters: the front gate oxide, film and BOX thicknesses were 308, 889 and 4000 Å, the channel doping was $2 \times 10^{16} \text{ cm}^{-3}$ only, and the channel length and width were $L = W = 20 \mu\text{m}$. Temperature measurements were performed up to 300 °C. Due to low doping of the Si film, we have the case of fully-depleted AM SOI pMOSFET.

Using the model, it is possible to find values of device parameters by fitting the model curve to experimental data. For this aim, the method of Fast Simulated Diffusion was used [13], especially developed for resolving of multidimensional minimization problems like MOSFET modeling is. The found values of main parameters at room temperature are shown in Table. The model also accounts the effect of decreasing the device length and width during technological processes of device manufacturing, *i.e.*, doping of the source and drain region and forming the side oxides. The appropriate corrections, lateral diffusion length for the channel length, and diffusion width for the width were determined and listed in Table.

In Fig. 3, we demonstrate the comparison of the experimental and model curves of the transistor transfer characteristics ($I_d V_g$) at room temperature both in linear (drain voltage $V_{ds} = -0.05 \text{ V}$, see Fig. 3a) and saturation ($V_{ds} = -2 \text{ V}$, see Fig. 3b) regimes of operation for different back-gate bias voltages. In Fig. 4, we compare the same curves in the logarithmic scale to see the results of modeling in the subthreshold region. It is clearly seen that the model shows a good agreement with

measurements in all the regions from subthreshold (Fig. 4) to above threshold voltages (Fig. 3) both in linear and saturation regimes.

Table. Determined values of MOSFET parameters and their temperature dependences.

Parameter	Room-temp. value	Temperature dependence(11) (parameters refitted)
Weak accumulation threshold voltage, $V_{th0,i}^r, \text{ V}$	-0.38	$V_{th0,i} = V_{th0,i}^r + 10^{-3}(T - T_{room})$
Strong accumulation threshold voltage, $V_{th0}^r, \text{ V}$	-0.41	the same
Hole mobility, $\text{m}^2/(\text{V}\cdot\text{s})$		
- in accum. channel, μ_{ac0}	0.0211	$\mu = \mu_0(T/T_{room})^{-1.6}$
- in body channel, μ_{b0}	0.0291	
Field mobility degr. factor, $\alpha_{f0}, \text{ m/V}$	1.65×10^{-8}	$\alpha_f = \alpha_{f0}(T/T_{room})^{-2.05}$
Lateral diffusion length, $l_{lat}, \text{ m}$	8.68×10^{-7}	
Diffusion width, $w_d, \text{ m}$	1.16×10^{-6}	
Source/drain series resist., $R_{tot}, \text{ Ohm}$	220	
Saturation rate, $v_{sat0}, \text{ m/s}$	8.0×10^4	$v_{sat} = v_{sat0} \frac{1 + 0.8 \exp(1/2)}{1 + 0.8 \exp(T/2T_{room})}$
Characteristic length, $l_d, \text{ m}$	2.09×10^{-8}	
Generation lifetime, $\tau_{g0}, \text{ s}$	0.9×10^{-7}	$\tau_g = 10^{-13} T^{2.4} \cosh(1.13 \times 10^{-6}/T)$
Recombination lifetime, $\tau_{r0}, \text{ s}$	0.1×10^{-6}	$\tau_r = \tau_{r0}(T/T_{room})^{2.7}$

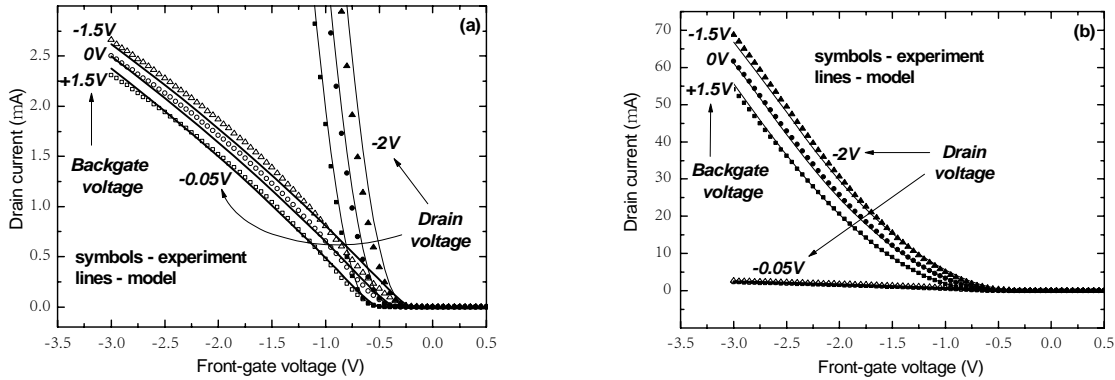


Fig. 3. Results of modeling the transfer characteristics ($I_d V_g$) at room temperature for various back-gate biases in the linear (a) and saturation (b) regimes.

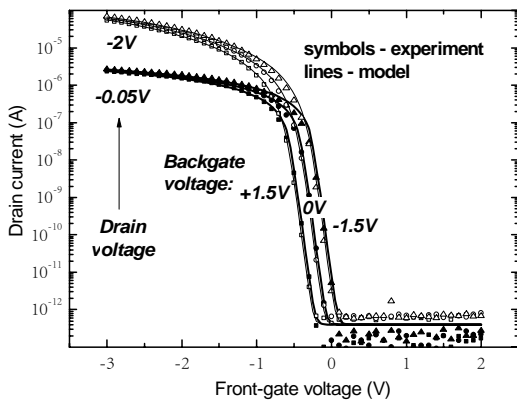


Fig. 4. Transfer characteristics ($I_d V_g$) at room temperature for various back-gate biases in the subthreshold region.

In Fig. 5, we compare the model and measured output characteristics ($I_d V_d$) at room temperatures. One can observe a good agreement for all the regimes of operation, from the linear to saturation ones.

3.2. High-temperature simulations

With regards to the main result of this work, *i.e.*, modeling the high-temperature AM MOSFET characteristics, the temperature dependences of the main model parameters are presented in Table.

Fig. 6 shows a comparison of the measured and model $I_d V_g$ curves for AM SOI pMOSFET at high temperatures. As one can see, modeled characteristics show a good agreement with experimental results in the wide range of temperatures (from the room temperature up to 300 °C) in linear (Fig. 6a) and saturation (Fig. 6b) regimes. A very important feature for analog design, *i.e.* the zero-temperature coefficient (ZTC) point, corresponding to a constant $I_d V_g$ bias point with temperature, is particularly well modeled, too.

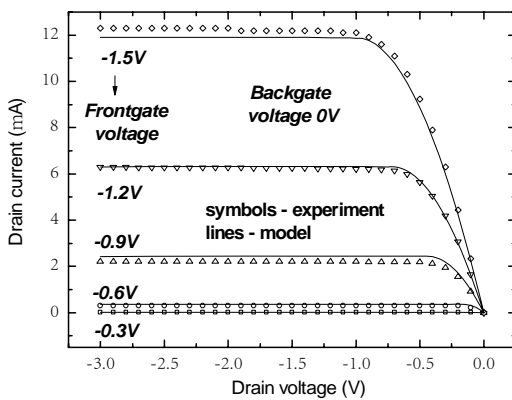


Fig. 5. The output characteristics ($I_d V_d$) at room temperature for zero back-gate bias.

The same characteristics, depicted in the logarithmic scale in Fig. 7a, show the behavior of the model curves in the subthreshold and off-state regions. As one can see, the subthreshold swing dependence upon temperature is very good. The model curves exhibit smooth transition between all the regimes of operation (from the off-state through subthreshold to the above threshold region). Also, the off-state current temperature dependence is correctly modeled. In Fig. 7b, we have more vivid picture of this dependence. The model curves demonstrate proper quantitative and qualitative description of the off-state current dependence upon temperature. As it should be expected, we have significant difference between the saturation and linear off-state currents at low temperatures, which is explained by increasing the generation current (30) at high absolute values of the drain voltage, because of increasing the depth of the depleted region near the drain [see Eq. (31)], where generation takes place. At the same time, the diffusion component of the off-state current (29) tends to saturate with the drain voltage. Concerning the temperature dependence of both components of leakage current, the generation component (30) increases with temperature as $n_i(T)$, while the diffusion one (29) varies as $n_i^2(T)$. At

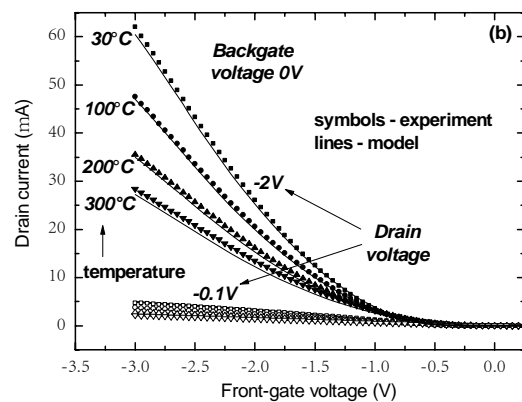
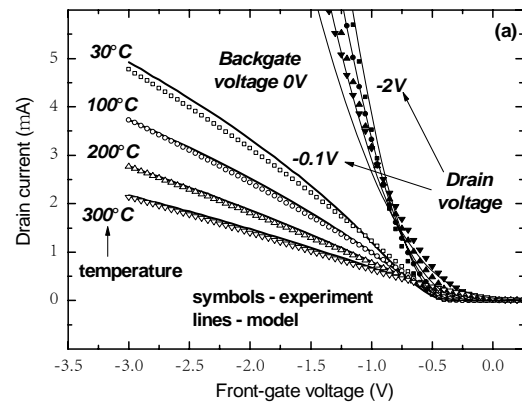


Fig. 6. Transfer characteristics ($I_d V_g$) at high temperatures for zero back-gate bias in the linear (a) and saturation (b) regimes.

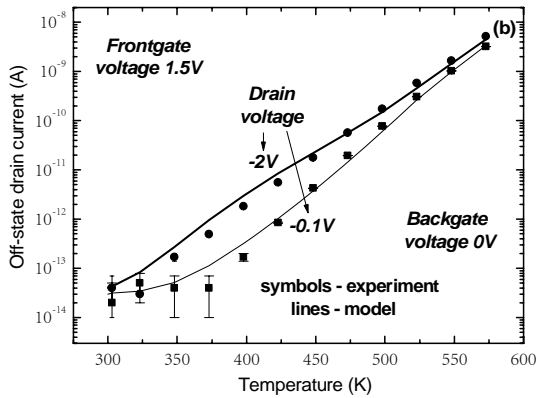
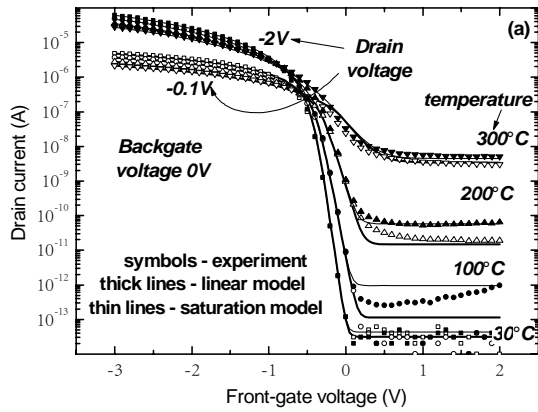


Fig. 7. Transfer characteristics ($I_d V_g$) at high temperatures for zero back-gate bias in the subthreshold region (a) and the off-state current vs temperature (b).

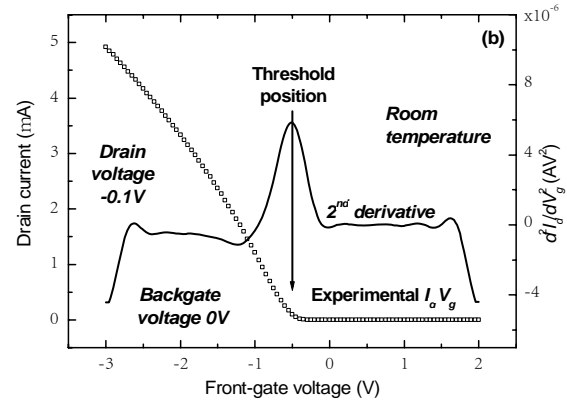
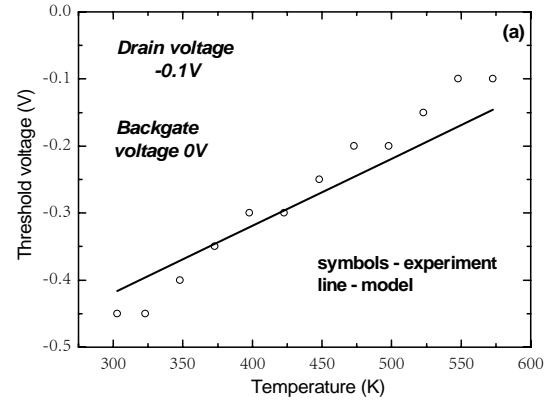


Fig. 8. Comparison of the experimental and model dependences for the threshold voltage upon temperature for zero back-gate bias (a) and an illustration of the 2nd derivative method for determining the threshold voltage (b).

high temperatures the diffusion current increases significantly, and it becomes the dominant component of the leakage current. Therefore, the difference between off-state currents in the saturation and linear regimes caused by the generation component becomes slighter at high temperatures, as clearly seen from Fig. 7b. The same feature of leakage current behavior at high temperatures was reported previously [12].

In Fig. 8a, comparing the experimental and model threshold voltage dependences upon temperature is presented. The experimental values of the threshold voltage were obtained from the experimental $I_d V_g$ curves by using the 2nd derivative method [14] (simple illustration of the method is depicted in Fig. 8b). Model curves are straight lines according to the chosen dependence of the threshold voltage upon temperature, and taking the dispersion of experimental values into consideration, model curves show a good coincidence with the experimental ones (Fig. 8a).

The important analog parameter g_m/I_d (g_m being the transconductance $g_m = dI_d/dV_{gf}$) for different temperatures is plotted in Fig. 9. When the value of

g_m/I_d is the largest ones, the maximum voltage gain of a MOSFET is obtained [7]. As Fig. 9a shows, the maximum of this parameter is getting lower with increase of temperature, due to the degradation of subthreshold operation, which infers that the maximum voltage gain of the device is significantly decreased. Nevertheless, when biasing the devices at the ZTC point, to maintain constant bias with temperature for analog circuits such as amplifiers [15], we observe and correctly model a much reduced degradation of the g_m/I_d coefficient with temperature (Fig. 9b).

The gate-source intrinsic capacitance ($C_{gs} = -dQ_g/dV_s$) measurements at the temperature 300°C compared to the model curves are plotted in Fig. 10. Experimental data were taken from the data for the transistor with the front gate oxide, film and BOX thicknesses of 550, 1000 and 4200 Å, the channel doping of $8 \times 10^{16} \text{ cm}^{-3}$, and with the channel length and width of 20 μm [4]. There is also a good agreement through all the regimes for different values of the drain voltage.

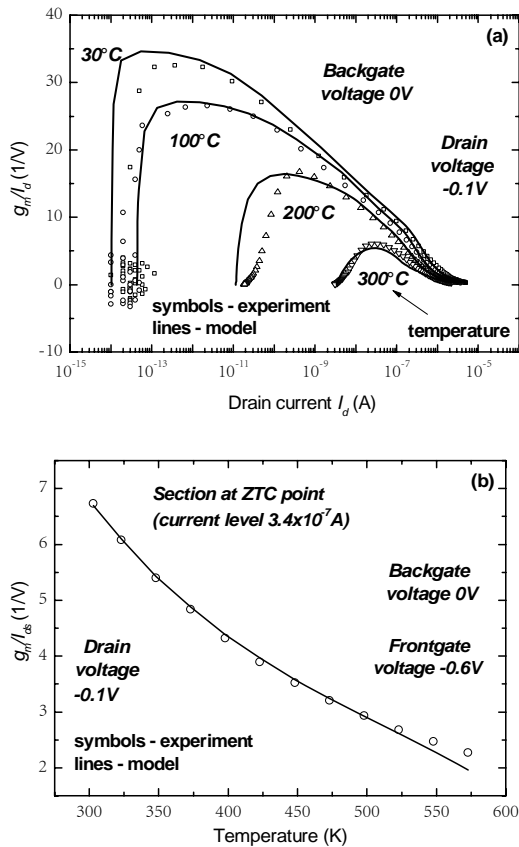


Fig. 9. Results of modeling the transconductance (g_m/I_d vs I_d) at high temperatures (a) and a section of this dependence at ZTC point (b).

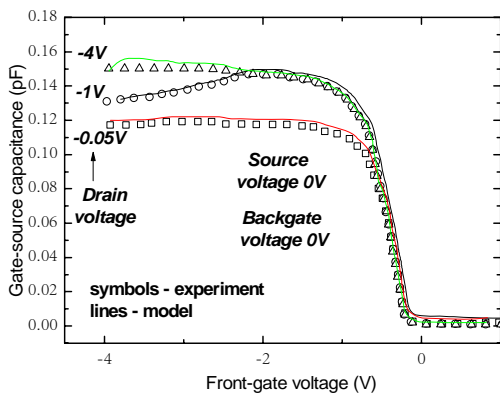


Fig. 10. Gate-source intrinsic capacitance (C_{gs} vs V_{gf}) at the high temperature (300 °C).

4. Conclusions

The high-temperature AM SOI *p*-MOSFET model has been developed in the paper. The model is based on the approximate C_∞ -continuous expressions of the

accumulation and quasi-neutral charge densities. The obtained agreement between the model and experimental data for AM SOI *p*-MOSFET characteristics is very good. We specifically developed new formulations for the subthreshold slope and off-state currents. The model works properly in all the operation regimes including subthreshold and off-state conduction in the range from the room temperature up to 300 °C. A smooth transition between different operation regimes, as well as proper modeling the AC and DC MOSFET characteristics (ZTC, transconductance-to-drain current ratio, intrinsic capacitances) is demonstrated, which allows to use the model for high-temperature analog circuits simulations.

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References

1. D. Flandre, S. Adriaensen, A. Akheyar, A. Crahay, L. Demeus *et al.*, Fully depleted SOI CMOS technology for heterogeneous micropower, high-temperature or RF Microsystems // *Solid State Electron.* **45**(4) p. 541–549 (2001).
2. B. Iñiguez, B. Gentinne, V. Dessard, D. Flandre, A physically-based C_∞ -continuous model for accumulation-mode SOI pMOSFET's // *IEEE Trans. Electron. Devices* **46**(12), p. 2295–2303 (1999).
3. B. Iñiguez, L. F. Ferreira, B. Gentinne, D. Flandre, A physically-based C_∞ -continuous fully-depleted SOI MOSFET model for analog applications // *IEEE Trans. Electron. Devices* **43**(10), p. 568–575 (1996).
4. B. Gentinne, D. Flandre, J.-P. Colinge, F. van de Wiele, Measurement and twodimensional simulation of thin-film SOI MOSFETs: Intrinsic gate capacitances at elevated temperatures, // *Solid-State Electron.* **39**(11), p. 1613–1619 (1996).
5. A. L. P. Rotondaro, U. K. Magnusson, C. Clayes, D. Flandre, A. Terao, and J.-P. Colinge, Evidence of different conduction mechanisms in accumulation mode p-channel SOI MOSFET's at room and liquid-helium temperatures // *IEEE Trans. Electron. Devices* **40**(4), p. 727–732 (1993).
6. J.-P. Colinge, Conduction mechanisms in thin-film accumulation-mode SOI p-channel MOSFET's // *IEEE Trans. Electron. Devices* **37**(9), p. 718–723 (1990).
7. J.-P. Colinge, *Silicon-On-Insulator Technology: Materials to VLSI*, 3rd edition. Kluwer Acad. Publ., Dordrecht (2004).
8. J.-P. Colinge, D. Flandre, and F. van de Wiele, Sub-threshold slope of long-channel accumulation-mode

- p-channel MOSFET's // *Solid-State Electron.* **37**(2), p. 289–294 (1994).
9. F. van de Wiele, A long channel MOSFET model // *Solid-State Electron.* **22**(12), p. 991–997 (1979).
 10. D. Flandre and A. Terao, Extended theoretical analysis of the steady-state linear behavior of accumulation-mode, long-channel p-MOSFETs on SOI substrates // *Solid-State Electron.* **35**(8) p. 1085–1092 (1992).
 11. D.-S. Jeon, D. E. Burk, A temperature-dependent SOI MOSFET model for high-temperature application (27 °C–300 °C) // *IEEE Trans. Electron. Devices* **38**(9), p. 2101–2111 (1991).
 12. T. E. Rudenko, V. S. Lysenko, V. I. Kilchytska, A. N. Rudenko, A comprehensive analysis of the high-temperature off-state and subthreshold characteristics of SOI MOSFETs, in: *Perspectives, Science and Technologies for Novel Silicon on Insulator Devices*, edited by P. L. F. Hemment, V. S. Lysenko, A. N. Nazarov. Kluwer Acad. Publ., Dordrecht, p. 281–293 (2000).
 13. T. Sakurai, B. Linn, A. R. Newton, Fast-simulated diffusion: An optimization algorithm for multimimum problems and its application to MOSFET model parameter extraction // *IEEE Trans. Computer-Aided Design* **11**(2), p. 228–234 (1992).
 14. H.-S. Wong, M. H. White, T. J. Krutsick, R. V. Booth, Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET's // *Solid-State Electron.* **30**(9), p. 953–968 (1987).
 15. J.-P. Eggermont, D. De Ceuster, D. Flandre, *et al.*, Design of SOI CMOS operational amplifiers for applications up to 300 °C // *IEEE Journal of Solid-State Circuits* **31**(2) p. 179–186 (1996).