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Optimization of technological parameters of ohmic contact junctions for GaAs-AlGaAs-based transistor structures

R.V. Konakova, V.V. Milenin, M.A. Stovpovoi

Institute of Semiconductor Physics, NAS of Ukraine, 45 prospect Nauky, 03028 Kyiv, Ukraine
Phone.: +380 (44) 265-6182; fax: +380 (44) 265-8342; e-mail: konakova@isp.kiev.ua

Abstract. The work deals with study and optimization of the technological parameters of ohmic contacts for HEMTs. It is shown that the depth of fusion front penetration into semiconductor is the main factor that determines ohmic properties of contact junctions.

Keywords: ohmic contact, contact resistance, GaAs-AlGaAs heterostructure.

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1. Introduction

It is known that field-effect transistors with modulated doping demonstrate high transconductance and small switching time at low dissipated power, low noise factor. The above characteristics are related primarily to high electron mobility and saturation rate of two-dimensional (2D) electron gas (EG). At low (below 100 K) temperatures the mobility increases abruptly. This results in a considerable growth of the device transconductance and decrease of the noise factor [1, 2].

However, the measured conductivity is less than the "intrinsic" one, and the noise factor is bigger due to a parasitic source resistance. That is why, along with optimization of the device construction (doping levels and layer thicknesses, gate self-alignment technology), optimization of the ohmic contact technology (i.e., provision of its lowest resistance) is needed to obtain high conductivity and low noise factor.

The objective of our work was to obtain the lowest source resistance, as well as determination of the critical optimization parameter for thermal treatment of the ohmic contact.

2. Sample preparation technique

The GaAs-AlGaAs heterostructures were formed using molecular-beam epitaxy. The electron mobility in the 2D EG was ~4000 $cm^2/V{\cdot}s$ at 300 K and about 40000 $cm^2/V{\cdot}s$ at 77 K. The heterostructure parameters are given in Table 1.

The ohmic contact outline was obtained using lift-off lithography. It is characterized by minimal effect of technological process on semiconductor surface. Immediately before metallization deposition the upper layer of n^+-GaAs was etched off in the ohmic contact windows. The depth of etching was no more than 4-5 nm because the thickness of n^+-GaAs upper layer was small.

For experimental samples we used eutectic AuGe alloy (88:12) 50 nm thick and Au (about 100 nm thick) as metallization. The samples were fused in the diffusion oven in the hydrogen atmosphere at a temperature of 430 °C for 25 s (group 1) and 35 s (group 2).

Table 1. The parameters of heterostructure layers (width d and electron concentration *n*).

Layer	*d*, nm	*n*, cm^{-3}
n^+-GaAs	60	$(1\div2)\times10^{18}$
n^+-AlGaAs	50	$(1\div2)\times10^{18}$
n-AlGaAs	3	10^{15}
n-GaAs	500	10^{15}
n-GaAs	3×10^5	10^{15}

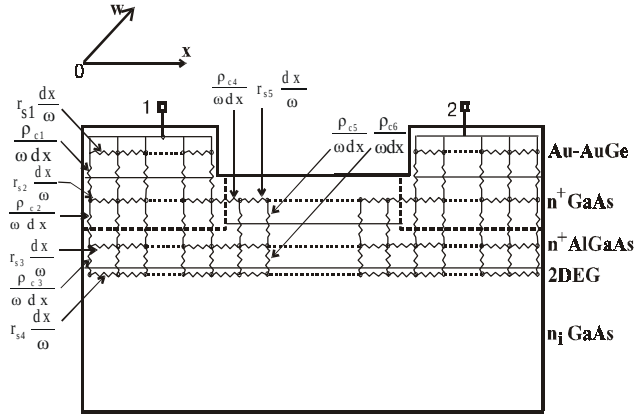

Fig. 1. Structure and equivalent circuit of ohmic contact (the spacer is not shown): r_{s1} – surface resistance of metallization layer; r_{s2} - surface resistance of fused layer; r_{s3} - surface resistance of n^+-AlGaAs layer; r_{s4} - surface resistance of 2D EG layer; r_{s5} - surface resistance of n^+-GaAs layer; ρ_{c1} - metal-fused layer contact resistance; ρ_{c2} – fused layer-n^+-AlGaAs layer contact resistance; ρ_{c3} - n^+-AlGaAs layer–2D EG layer contact resistance; ρ_{c4} – fused layer n^+-GaAs layer contact resistance; ρ_{c5} - n^+-GaAs layer–n^+-AlGaAs layer contact resistance; ρ_{c6} - n^+-AlGaAs layer–2D EG layer contact resistance.

3. Results and discussion

A sketch of ohmic contact (at such thermal treatment mode that the fused layer boundary penetrates to the middle of the n^+-AlGaAs layer) and its equivalent circuit are given in Fig. 1. Each layer (interface) is schematically presented as a distributed surface (contact) resistance. The values of resistances $r_{s3}dx/w$, $r_{s4}dx/w$, $r_{s5}dx/w$, ρ_{c3}/wdx, ρ_{c5}/wdx, ρ_{c6}/wdx are mostly determined by the parameters of the starting semiconductor structure. Their dependence on the technological process used for the ohmic contact formation is slight. This dependence is determined by the lateral diffusion resulting in narrowing of the gap between the contacts 1 and 2.

A typical value of the gap (source-drain spacing) is about 3 mm (for low-noise microwave FETs) or 4 μm (for high-power transistors), while the lateral diffusion length is 80 nm (as was shown in [3]). The values of resistances $r_{s1}dx/w$, $r_{s2}dx/w$, ρ_{c1}/wdx, ρ_{c2}/wdx, ρ_{c4}/wdx depend on the electrophysical characteristics of metallization, starting semiconductor structure and (most strongly) on the modes of thermal treatment used when forming ohmic junctions. The relative contributions from the equivalent circuit resistances to the total resistance value are different.

Our heterostructure had heavily doped GaAs upper layer, so the technology of ohmic contact formation was similar to the well-known (see, e.g., [4, 5]) technology of formation of ohmic contacts to GaAs. It is known that the resistances of metallization ($r_{s1}dx/w$) and fused layer ($r_{s2}dx/w$), as well as that of the metal-fused layer contact

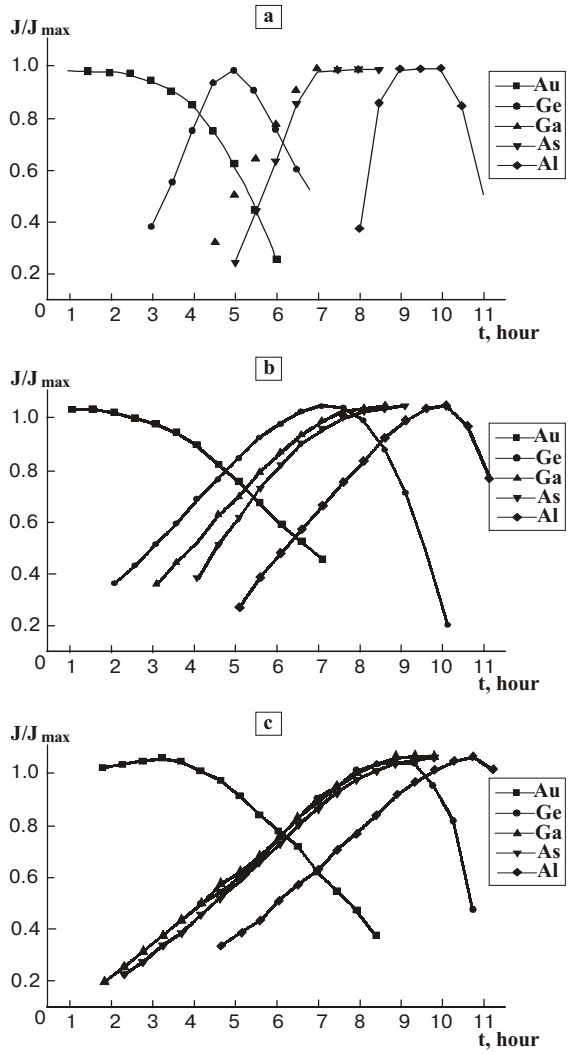

Fig. 2. Auger concentration depth profiles of the heterostructure components: a – immediately after metallization deposition; b and c – after thermal treatment at 430 °C for 25 and 35 s, respectively.

(ρ_{c1}/wdx), are low as compared to the fused layer-n^+-AlGaAs (ρ_{c2}/wdx) and fused layer-n^+-GaAs (ρ_{c4}/wdx) resistances [6, 7]. The n^+-AlGaAs layer resistance ($r_{s3}dx/w$) is high as compared to those of the 2D EG and n^+-GaAs layers ($r_{s4}dx/w$ and $r_{s5}dx/w$, respectively). The reason for this is that the n^+ AlGaAs is fully depleted, and charge carrier mobility is low in it [8]. So one can assume that the source resistance essentially depends on the location of the fused layer-semiconductor interface.

By choosing proper mode of thermal treatment after metallization deposition, it is possible to make this interface (the fusion front determined from the dopant penetration depth) to reach the localization layer of 2D EG. In this case the contact resistance could become minimal. Thus the technological problem how to form ohmic contact to heterostructure is reduced to selection of such thermal treatment mode which would provide (i) fusion front penetration to the 2D EG layer and (ii) minimal contact

resistance. Below is shown that the first condition is the crucial factor for obtaining the minimal source resistance.

The above conclusions have been supported experimentally using the layer-by-layer Auger analysis and measurements of the contact junction resistance. Shown in Figs. 2a, 2b, 2c are the Auger concentration depth profiles for the heterostructure components taken immediately after metallization deposition and after thermal treatment (fusion at 430 °C for 25 and 35 s). These results (see Fig. 2b) evidence that after thermal treatment at a temperature T = 430 °C for 25 s the fusion front reaches depth of 70-80 nm. (The fusion front is arbitrarily defined as corresponding to the depth where intensity of Ge signal is half its maximal value.) This is in the vicinity of the middle of the n^+-AlGaAs layer. Thermal treatment for 35 s results in further Ge and Au diffusion into the semiconductor bulk. In this case (T = 430 °C, fusion duration of 35 s) the fusion front reaches depth of 100-110 nm. This is in the region where the 2D EG layer is localized (see Fig. 2c). One should also note intense Al, Ga and As diffusion to the metal film surface. This fact indicates at low thermal stability of the contact structures studied. It seems that one should use antidiffusion barriers to improve their thermal stability.

The results obtained with the Auger layer-by-layer analysis are in good agreement with those obtained by measuring the contact structure resistances. When measuring contact resistivity ρ_c, we used the standard technique [9]. It was found that ρ_c was about 1.5×10^{-6} $\Omega\cdot cm^2$ for the samples belonging to the first group and about 6×10^{-6} $\Omega\cdot cm^2$ for those from the second group. Below is shown that the c_c contribution to the total resistance of ohmic contact is small, so the value ρ_c = (3-8)$\times10^{-6}$ $\Omega\cdot cm^2$ seems to be quite plausible.

Our estimation of the contact resistance R_c gave the following results: R_c = ~0.02 Ω (group 1) and ~ 0.15 Ω (group 2). At the same time the total (source-drain) resistance was, correspondingly, 8 Ω (group 1) and about 6 Ω (group 2). Thus for the samples from group 1 the resistances of n^+-AlGaAs and n-AlGaAs (spacer) layers that are between the fusion front and 2D EG layer are about 2 Ω. This is two orders of magnitude bigger than the contact resistance. Therefore the main contribution to the total resistance of the contact junction comes from the n^+-AlGaAs and n- AlGaAs layers and not from the fused layer-semiconductor interface.

4. Conclusion

We have shown experimentally that the main factor affecting contact structure resistance is depth of Ge front penetration into semiconductor, and not the contact resistivity. Starting from this conclusion, we have refined technological procedure for obtaining ohmic contact to the GaAs-AlGaAs heterostructure with minimal contact structure resistance.

References

1. M. Shur, *GaAs Devices and Circuits*, Plenum Press, New York and London (1987).
2. GaAs Microelectronics (*VLSI Electronics Microstructure Science,* v. 11), Eds. N.G. Einspruch, W.R. Wisseman, Academic Press, New York (1985).
3. V.I. Osinskii, M.A. Stovpovoi, Study of planar contacts to the quantum-sized nanolayers of n-GaAs-n-GaAs-n-GaAlAs- n^+-GaAlAs-n^+-GaAs heterostructures // *Optoelektronika i Poluprovodnikovaya Tekhnika*, **29**, pp.18-24 (1995) (in Russian).
4. Yu.A. Goldberg, Metal-$A^{III}B^V$ semiconductor ohmic contact: formation techniques and properties // *Fiz. Tekh. Poluprov.*, **28**(10), pp.1681-1698 (1994) (in Russian).
5. A. Piotrowska, A. Guivarc'h, G. Pelous. Ohmic contacts to III-V compound semiconductors: A review of fabrication techniques // *Solid-St. Electron.*, **26**(3), pp.179-197 (1983).
6. GaAs FET Principles and Technology, Eds. J.D. DiLorenzo, D.D. Khandelwal, Artech House, Inc. (1984).
7. S.J. Lee, C.R. Crowell, Parasitic source and drain resistance in high-electron-mobility transistors, Solid-St. Electronics, 28(7), pp.659-668 (1985).
8. K. Ikossi-Anastasiou, A. Ezis, A. Rai, Temperature dependence of transient and conventional annealed AlGaAs/GaAs MODFET ohmic contacts // *IEEE Trans. Electron Devices*, ED-35(11), pp.1786-1792 (1988).
9. S.N. Madayan, M.P. Guseinkhanov, Resistivity measurements for ohmic contacts with a thin semiconductor layer // *Izv. Vuzov. Fizika*, No 6, pp.80-83 (1976) (in Russian).