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The effect of doping methods on electrical properties and micromorphology of polysilicon gate electrode in submicron CMOS devices

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Abstract. Two doping methods for introducing phosphorus atoms into polysilicon to form a gate electrode for 0.5 μm CMOS were investigated. These methods were ion implantation and the "in-situ" one (it is also known as thermal diffusion). For the in-situ method, the concentration of $1.8 \cdot 10^{20} cm^{-3}$ for Si_2H_6 and phosphane (PH_3) were used, in the course of ion implantation applying two different doses: $2.0 \cdot 10^{16}$ and $3 \cdot 10^{16} cm^{-2}$ at 40 keV. The micromorphology of the polysilicon surface was studied using the atomic force microscopy (AFM). The polysilicon thickness obtained via the in-situ method ranged between 12.35 and 26.08 nm, with an average value thickness of 18.0 nm, and its sheet resistance value was 21±1 ohm/square. As for the ion implantation method, at the lower doses the thickness ranged at about 12.00 upto 46.0 nm with an average value of 24.0 nm, and its sheet resistance values were of 36±13 and 45±21 ohm/square, respectively. At the higher doses, the thickness varied from 12.16 to 47.84 nm with an average meaning 23.96 nm, and its sheet resistance value was between 25 to 40 ohm/square. Therefore, polysilicon doped by the in-situ method has smoother and thinner surface and possesses better electrical properties.

Keywords: polysilicon gate, micromorphology, ion implantation.

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1. Introduction

The gate structure of the CMOS devices has not changed dramatically in the past several years. The most common choice of gate materials for modern devices is a layered structure of polysilicon with metal silicide on top of the gate. Heavily doped polysilicon films are used to form the gate conductor in MOSFETs, as a dopant source for contacts of very shallow junctions in high-speed bipolar transistors and MOSFETs, as a conductive layer for interconnections, and for electrically trimable resistors. At a moderate to low dopant concentrations polysilicon is used for high value resistors and capacitors in analog designs, and thin-film transistor (TFT) [1,2]. Different methods of doping and annealing procedures have been introduced to improve the thermal diffusion process in order to find the better way in producing the precise distribution of impurities in which a better electrical characteristics of polysilicon films successfully tailored into specific application [3]. Ion implantation is another alternative technique of introducing such impurities into polysilicon with a more precise manner. The dopant atom is fired into the polysilicon surface through accelerated ions with energies 20 to 200 keV [4]. Even though the thermal diffusion is well established for VLSI production, the ion implantation offers a few advantages. The latter provides a better lateral registration of doped regions and superior control of dopant concentration, depth and uniformity. The fact that repeatability of surface concentrations of $10^{16} cm^3$ or less and uniformity at these low concentrations is easier to achieve with ion implantation compared to ordinary thermal diffusion process at high temperature.

In CMOS processes particularly, one of the main reasons for using the polysillicon is due to the fact that polysilicon allows the integration of "dual-flavoured"

gates: *p*- and *n*- type polysilicon for PMOS and NMOS, respectively. Grain sizes and the surface texture of these films are functions of the polysilicon deposition and doping conditions as well as subsequent oxidation and thermal cycles [1, 2]. The top surface roughness of the polysilicon might not be important for the conventional devices. However, it is of great importance in advanced three-dimensional (3D) complementary MOS (CMOS), BiCMOS [3, 4], and for multilevel dielectrics. In these 3D devices, selective epitaxial lateral growth (SEG) and epitaxial lateral growth (ELG) were used to grow single crystal silicon on top of the existing polysilicon gates (polygate) protected by a thermal polyoxide. It is necessary to minimize the roughness of the polysilicon top surface and the roughness of the polyoxide when ELO silicon is grown on top of the structure that serves as a second MOSFET. In this 3D CMOS structure, the shared gate is sandwiched between the *n*-MOS and *p*-MOS devices. The interface must be smooth to reduce carrier scattering and its state density, as well as potential defect generation in the ELG silicon [5].

In this work, the micromorphology of the polysilicon gate for 0.5 mm CMOS devices doped with phosphorous using both methods aforementioned: the *in-situ* and ion implantation are presented. The analysis of the micromorphology were afforded by using AFM images which provide the thickness measure of the polysilicon layer. The study of electrical properties, namely sheet resistance measurements of the sample, were done using spread resistance technique.

2. Experimental procedure

The thermal diffusion method for the 0.5 mm CMOS fabrication process involves the use of twelve N-type phosphorous doped CZ silicon wafers of 100 mm in diameter and with <100> orientation. First, the wafers were coated with resist of 1.48 μm thickness. Then, they were developed in the developing solution for 60 seconds and subsequently etched with HF/HNO_3. All wafers used were subjected to a standard RCA cleaning procedure. Next, a group of four wafers were formed and numbered as wafer 1 to 4, loaded into the vertical furnace for oxide growth and undergo the thermal drying oxidation process at 900°C for 22 minutes. The four wafers (i.e. wafers no. 1-4) were then transferred back into the vacuum chamber for preparation of the 3000°A polysilicon gate electrode by the low-pressure chemical vapor deposition (LPCVD) technique using Si_2H_6 gas with concentration of $1.8 \cdot 10^{20} cm^{-3}$ and phosphane (PH_3). Next, the other eight wafers, representing wafer numbers 5 to 12, were deposited with the undoped silicon (3000°A thickness) also by the LPCVD technique using SiH_4 gas instead. Finally, all wafers are again cleaned with resist of 1.48 μm thickness, followed by backside etching and ashing, to remove all traces of resist remains at the back of the wafers.

As for the ion implantation method, the wafers are cleaned with a special chemical called 'piranha' before performing the ion implantation process. This is to remove any contaminant and impurities that will contribute to the formation of long life radioactivity that can create unwanted contribution to the electrical characteristics. Next, the wafers were bombarded with 40 keV phosphorous ions in an ion implanter. Two wafer sets, consisting of four each, were implanted at different doses of $2.0 \cdot 10^{16}$ ions/cm^2 (for wafer 5–8) and $3.0 \cdot 10^{16}$ ions/cm^2 (for wafer 9–12). The choice of doses was based on the pre-determined estimated data such that it will produce low conductance polysilicon to agree with the electrical characteristics shown by the in-situ doping process. The two-step annealing method was used in this study to analyse the radiation impacts on the final sheet resistance; namely, structural and impurities related impacts. The films was first annealed at 800^0C for 30 minutes in dry nitrogen to repair the structural damage due to ions collisions during implantation. The second annealing step was done at 950^0 C for 5 minutes in dry nitrogen to redistribute the impurities homogeneously throughout the films. Finally, the wafers were immersed in the buffer oxide etchant for 30 seconds, rinsed with deionized water (DI) and blow dried with dry nitrogen gas to remove the cap oxide layer.

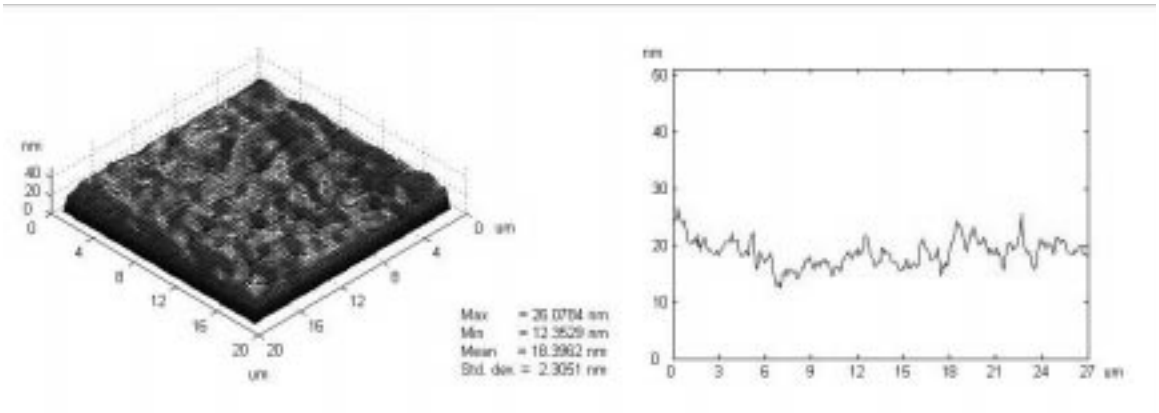
Sheet resistance measurements were done using four point probe based instrument of OmniMap Prometrix. It is a long established technique to measure the average resistance of a thin layer or a sheet by passing current through the outside two points of the probe and measuring the voltage across the inside two point [8].

In order to obtain the micromorphology of the polygate, the atomic force microscopy (AFM) machine of Digital Instrument Nanoscope III was used and also subjected to the image enhancing technique to improve the image resolution [9]. AFM machine, that is capable of imaging virtually any surface in three dimensions with scan areas ranging from a few atoms to tens of microns. The AFM machine was calibrated as mentioned in [10] prior to the analysis of samples. The instrument was located in such a way that it is free from any mechanical, acoustical and electrical noise or vibration.

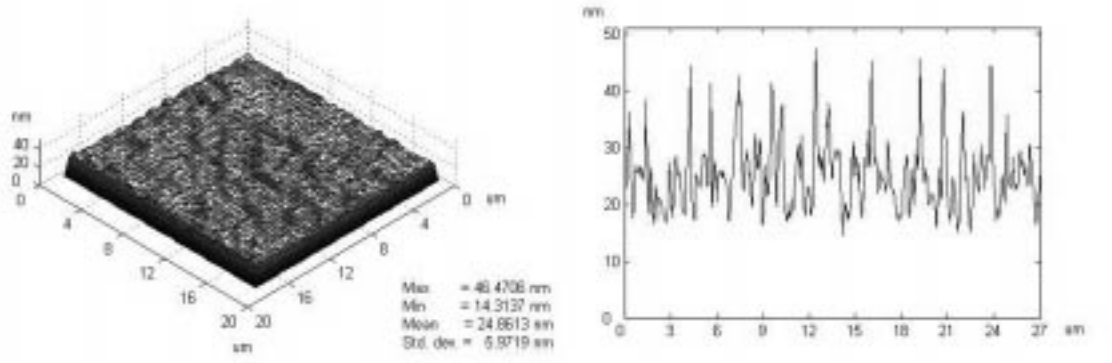
The samples were fixed to the stage ensuring that it does not tilt too much. The suitable load is between 10^{-8} to 10^{-9} N and the scanner was set to scan around the center of the x, y and z axes. The sheet resistance measurement was done using spreading resistance probe (SRP) of OmniMap Prometrix.

3. Results and discussion

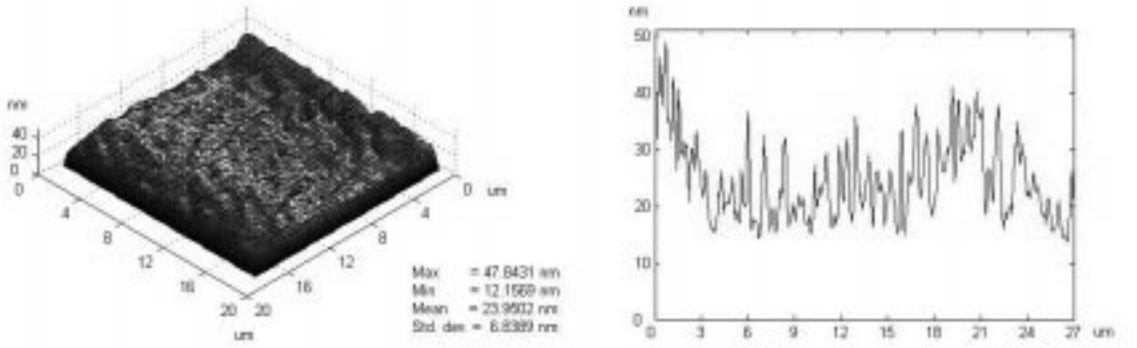
Results obtained are presented in Figs 1 and 2 as well as summarized in Table 1. Fig. 1 displays the plots of column pattern over the entire surface and its thickness profile, while Fig. 2 exhibits the relationship between the sheet resistance and the points of measurement on wafer obtained from the spread resistance probe (SRP) measurement. The wafer #4 prepared by *in-situ* doping of phosphane mixed with silane had sheet resistance value of around 21±1 ohm/square. The wafer # 11 and # 14 that



(a) Sample no. 4



(b) Sample no. 11



(c) Sample no. 14

Fig. 1. Plots of columns' patterns over the entire surface of the AFM images with their typical profiles for the sample No. 4, 11 and 14, respectively.

Table 1. Summary of results from the AFM images

Sample No.	Fabrication method	Surface Thickness from AFM Images (nm)			
		Max	Min	Average	Std. Dev
4	In-situ	26.0784	12.3529	18.3962	2.3051
11	Ion Implantation	46.4706	14.3137	24.8613	5.9719
14	Ion Implantation	47.8432	12.1569	23.9502	6.8389

were doped by the implantation method have their sheet resistance value of 36±13 and 45±21 ohm/square. The standard deviations of 13 and 21 are very significant values. These indicate that the variation of the value is too high and hence, reflect the uncertainties or inconsistence.

The AFM images of the polysilicon wafer of the sample no. 4 are shown in Fig. 1(a). While the AFM polysilicon images of samples 11 and 14, implanted by phosphorus ions, are shown in Fig. 1(b) and 1(c), respectively.

The AFM images of each sample are processed and analysed to determine the surface micromorphology of the microstructures. The AFM images are digitally converted and processed using the image processing toolbox of MATLAB. Image analysis of the microstructure surface of sample 4 indicates that the surface thickness varies from 12.3529 to 26.0784 nm with an average thickness of 18.3962±2.3051 nm. For the sample no. 11, the thickness varies from 14.3137 to 46.4706 nm with the average thickness of 24.8613±5.9719 nm, while for the sample no. 14 the thickness varies from 12.1569 to 47.8432 nm with the average thickness of 23.9502±6.8389 nm which is rather rough compared to the sample no. 4.

The two steps annealing process were introduced as means for repairing the radiation damage, and improving activation by redistributing the impurities. In this work, using a low temperature furnace, the first annealing step was able to sweep out point defects while the subsequent annealing step was able to activate the dopants [11]. However, we have used higher annealing temperature since the implantation process was done at higher energy ion beams.

The polysilicon gate electrode is modeled either as a perfect conductor or as a heavily doped single-crystal silicon [12]. We have observed that the electrical conductivity is improved when the grain size is larger, as in the case of the polysilicon doped by in-situ method. Referring to Fig. 3 and comparing all three surface micromorphology of samples 4, 11 and 14, it is observed that wafer sample 4 has smoother surface than samples 11 and 14. Thereby, it can be concluded that the sample 4, which is the thinnest wafer, has better thickness control compared to samples 11 and 14. In addition, the sample no. 4 has the better value of sheet resistance as shown in Fig. 2.

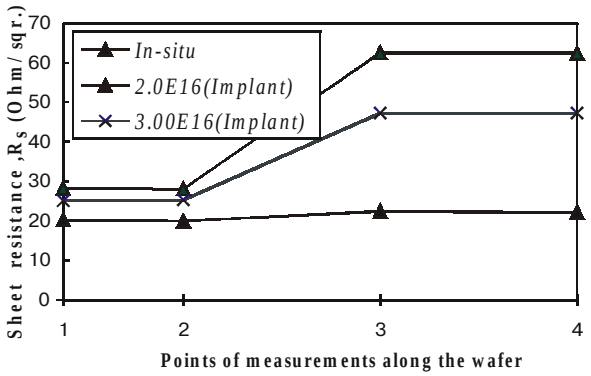


Fig. 2. Sheet resistance vs. points of measurements along the wafer

4. Conclusion

In this work, the influence of doping techniques and impurities factors on polysilicon films has been studied using AFM images. We found that both factors have strong influence on the electronic properties of the films [13,14]. We have shown that polysilicon doped with phosphane (PH_3) by *in-situ* produces very thin wafer compared to samples developed by the ion implantation method. It can be concluded that polysilicon film doped by the *in-situ* method has smoother surface and better thickness control than the implantation method implying better electrical conductivity. We also found that the AFM image analysis is a very useful tool for determining the surface micromorphology especially for submicron devices.

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