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Effect of oxide-semiconductor interface traps on low-temperature operation of MOSFETs

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Abstract. Operation of *n*-channel MOSFET was studied at low temperatures. It has been shown that the charge state of shallow traps in the Si/SiO_2 interface is responsible for the hysteresis of transistor drain characteristics in the prekink region. Thermally activated emptying of these traps leads to the sharp decrease of the current in the subthreshold mode of transistor operation

Keywords: low temperature, MOS transistor, hysteresis, shallow traps.

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1. Introduction

A large number of papers were devoted to investigations of hysteresis, transient, long-term drift and kink effects that are inherent to operation of MOSFETs at cryogenic temperatures (4.2-25 K) [1–4]. Kinks in the output characteristics are well explained by the effect of substrate freeze-out [1, 3], but there was no clear understanding of pre-kink transient behaviour. Several physical mechanisms have been proposed to explain transient behaviour observed at deep cryogenic temperatures. Positive transients (an increase of the drain current I_D with time) were explained by the increase in the electron mobility. Another kind of transients was related to the slow ionization of the frozen-out dopants in the substrate. It has been demonstrated that at $T > 10$ K Poole-Frenkel-assisted thermal ionization generates a slow buildup of the depletion charge in the substrate, causing a decay in I_D [5]. It was noted in [3] that this mechanism is very unlikely at 4.2 K, although transients are still observed at this temperature. So, we must agree with authors of papers [2, 4] that no satisfactory model exists to describe the prekink hysteresis behaviour.

In this paper we study the low-temperature operation of *n*-channel MOSFETs in the prekink region and suggest a model explaining the long-term hysteresis effects by slow recharging of traps in the transition Si/SiO_2 layer.

Extensive studies have shown that the interface between silicon and its thermal oxide can not be presented as an interface between an ideal crystal and a perfect amorphous material with a sharp boundary of atomic scale [6, 7]. Investigations of the structure of Si/SiO_2 interface revealed the presence of thin transition layer with thickness of few Angströms. The presence of a specific structure of the transition layer with distorted Si-O-Si bond-angles was found even in the case of ultrathin SiO_2 layers fabricated on silicon substrates in a quite uniform oxidation process [8]. The structural disorder in the transition layer leads to appearance of shallow centres in the dielectric [9]. Measurements of thermally stimulated charge release (TSCR) currents carried out in MOS structure [10, 11, 12] have shown that two systems of transition layer centres exist near conduction and valence band edges. The carrier exchange between them and the respective allowed silicon bands is controlled by a tunnel-activation mechanism. The activation energies of the carrier release from these traps range between 10 and 45 meV, and their emptying takes place at temperatures from 8 to 18 K. The recharging of these centres may be at the origin of the low-frequency (1/*f*) noise and of the random telegraph signal in small MOSFETs [13].

The aim of this paper is to show that recharging of these centres may be one of possible mechanisms responsible for hysteresis effects observed in *n*-channel MOSFETs at temperatures below 20 K.

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2. Experimental

Enhancement mode *n*-channel transistors were fabricated using a standard technology on *p*-type silicon substrate ($N_A = 10^{15}$ cm^{-3}). The backside was degenerately doped (for the substrate contact). Transistors with the channel width to length ratio of 30 μm / 3 μm were studied. Gate oxide thickness was 45 nm. The adjustment of threshold voltage was not performed.

Charging of hole traps in the Si/SiO_2 interface was performed by application of a negative bias to the gate at temperature 23 K. The drain, source and substrate of the transistor were grounded during charging. Then the transistor was cooled to a lower temperature, the charging bias was turned off and working biases were applied to its terminals. The output transistor characteristics (I_D vs. V_D) were measured prior to and after trap filling with the rate of drain voltage sweep 0.05 V/s. In measurements, as a rule, low drain bias V_D was used (from 40 to 200 mV) to avoid impact ionization, avalanche breakdown and hot carrier effects. The transient behaviour of transistors with charged interface traps was studied also by measuring the drain current transients at different temperatures and by measuring the temperature dependencies of drain current while heating the transistor.

Another set of experiments was carried out on MOS capacitors fabricated on *p*-type silicon substrate with impurity concentration of 10^{15} cm^{-3}. Oxide thickness was 120 nm. For the metal (gate) electrode an aluminum film was deposited onto the oxide. Capacitor area was $5\cdot10^{-3}$ cm^2. In this case filling of the shallow TL centres was achieved by applying an accumulation bias (V_G<0) to the structure at a temperature 20 K or higher. If the structure is cooled after the charging to 6 K and then the gate voltage is reduced to zero, the structure will be turned in the non-equilibrium depletion mode since the holes will be captured in the interface traps. Charge emission may be performed in two ways. First, the conventional thermally stimulated charge release (TSCR), when at zero voltage the structure is being heated and the temperature dependence of the emission current is registered. The second way, suggested in [11], consists in a linear gate bias sweep from accumulation to depletion mode at constant emission temperature with registration of the dependence of the emission current on the gate voltage.

3. Results

The thermally stimulated current shown in Fig. 1 was measured in the structure where the set of gates of several transistors connected in parallel were used as a top electrode. Filling of traps was performed by applying the negative voltage to the gate at 20 K. It can be seen that the position and shape of the peak on the temperature scale are the same as observed earlier [10], where such peaks were attributed to the charge release from shallow traps situated in the transition Si/SiO_2 layer. Activation energies of these traps, determined from the initial slope of the TSCR peaks, are 18, 24 and 32 meV.

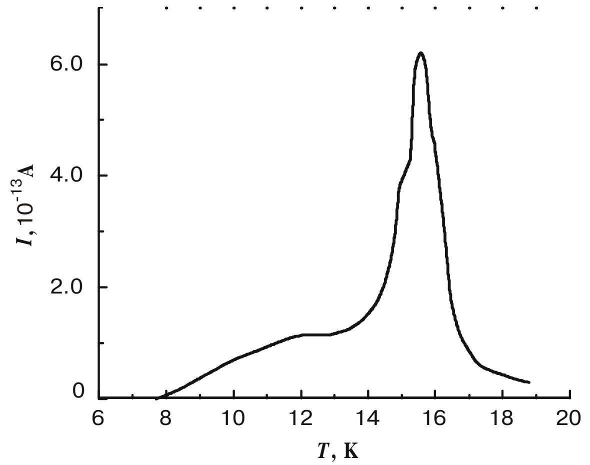

Fig. 1. TSCR current measured on «gate-SiO_2-pSi» structure after filling by a negative voltage at 20 K.

Fig. 2 shows drain characteristics of the transistor for different gate bias measured at 15 K for the cases of initially empty (open) and initially filled (full) interface traps. Traps were filled at 23 K with gate bias of –1 V. The output characteristics were measured in the strong inversion mode, at gate bias V_G higher than a threshold voltage. Threshold voltage V_T, as determined from the input characteristics, was equal to 0.41 V.

It can be seen that charging of hole traps, i.e. capture of positive charge near the «silicon-gate oxide» interface, results in an essential increase of the current in the initial part of the curve. This can be considered as an effective reduction of the threshold voltage by about 0.05 V. After reaching the definite value of drain bias, corresponding to the beginning of nonlinear mode of transistor operation, the I_D–V_D curves gradually approach to the respective curves for empty traps.

In Fig. 3 the hysteresis of output characteristics is shown as a function of the drain bias with a gate bias as parameter. The plots were obtained by subtraction of the reference curves with no trap filling from the respective curves with trap filling. For clarity all resulting plots were normalized by the maximum value of excess cur-

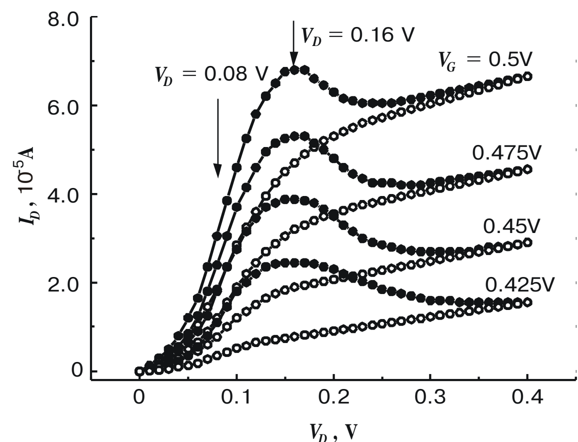

Fig. 2. Drain characteristics of the *n*-channel transistor at temperature 15 K for filled (full symbols) and empty (open) traps.

rent. Two conclusions can be drawn from these plots. First, the curves for different V_G coincide at drain voltage variation from zero up to V_D of about 0.15 V, corresponding to the maximum of hysteresis amplitude. Second, beyond the maximum, the extra current drop is faster for higher gate voltages.

The amplitude of the observed «hump» depends on the measurement temperature. In Fig. 4 the output characteristics are shown measured at different temperatures after filling the hole traps. In the inset respective hysteresis are shown. It can be seen, that the hysteresis amplitude is maximum at 10 K, slightly reduces with increasing temperature up to 15 K and falls rapidly in the range 16-17 K. At temperatures above 17 K the hysteresis is not observed. Relative independence of the hysteresis amplitude on temperature at temperatures below 15 K indicates that in this temperature region the «hump» is field-controlled.

The dependence of peak amplitude at 15 K on the filling voltage is shown in Fig. 5. The amplitude increases as the filling voltage increases, coming to saturation at voltages above –2.5 V. In this respect the «hump» manifests the same behaviour as that of TSCR peaks, where saturation in dependence on the filling voltage was also observed.

Since the extra current seems to be related to the charge state of hole traps, we have studied the isothermal transient currents of the transistor being switched on after preliminary filling the traps. Such measurements allowed us to study the kinetics of charge release in dependence on temperature and transistor operation mode. In this case, after filling the hole traps the transistor was turned on, and the drain current was measured as a function of time at a fixed temperature. Transient currents were measured in two modes, the first one, corresponding to the linear (or Ohmic) mode of transistor operation (V_D = 0.08 V) and the second one, corresponding to the nonlinear mode (V_D = = 0.16 V). These values of drain bias are indicated by arrows in Fig. 2. It can be seen, that at V_D = 0.16 V the maximum hysteresis amplitude is achieved, and with further increasing V_D the hysteresis decreases.

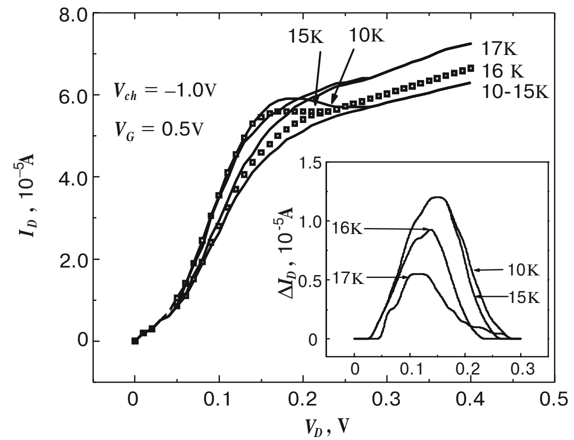

Fig. 4. Drain characteristics measured at different temperatures (indicated in the figure). Inset shows the respective hysteresis.

In Fig. 6 the transistor's transient behaviour in the linear operation mode is shown. It can be seen in the figure that in Ohmic mode the transients are described by an exponential relaxation low. At temperatures below 14 K time constant t is very long, that is, the current practically does not change during the measurement time. The Arrhenius plot of time constant τ (see insert) is a straight line in the temperature range 15–17 K indicating that the relaxation process is controlled by thermal activation. The respective activation energy was found to be equal to 30 meV. The excellent agreement of both the temperature range and activation energy values should be noted with those reported from TSCR measurements.

Fig. 7 shows the same plots for the nonlinear part of the output characteristic. It can be seen that transient times in this mode become much shorter, and the relaxation process can not be longer described by the exponential law. The rapid acceleration of the transient processes is related to the onset of the field mechanism of the trapped charge release, as will be shown below.

In Fig. 5 the temperature dependencies of the transistor drain current in the subthreshold mode are shown for

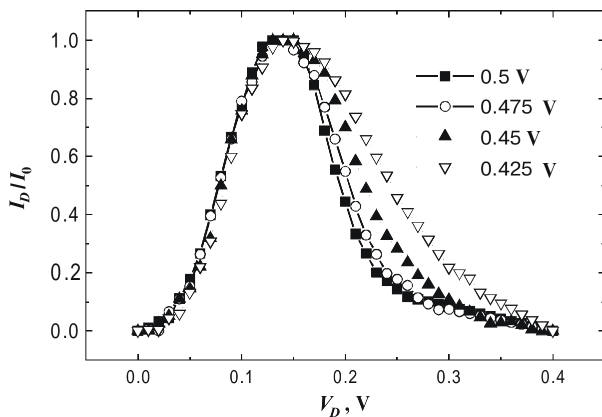

Fig. 3. Drain current hysteresis at different gate voltages (indicated in the figure).

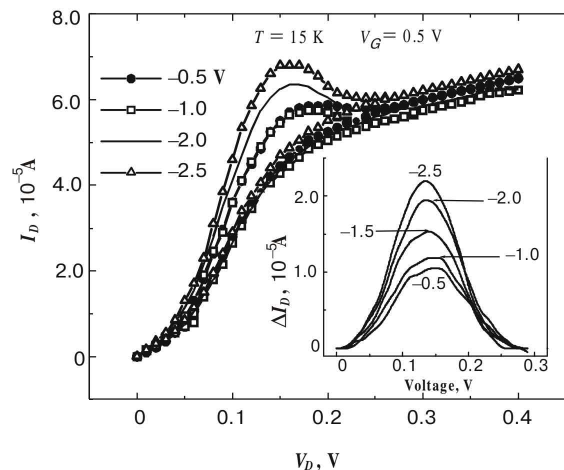

Fig. 5. Drain characteristics measured after filling with different charging voltage. In the inset respective hysteresis are shown.

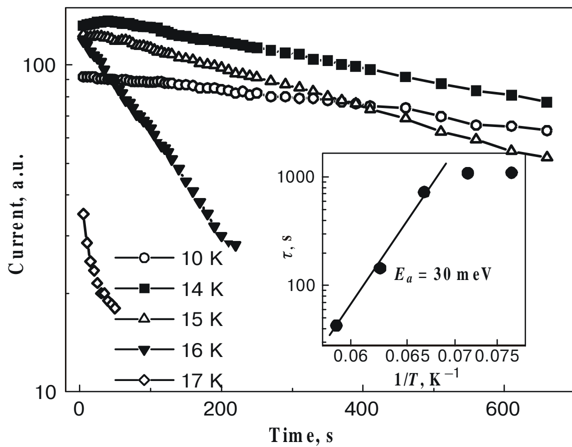

Fig. 6. Transient behaviour of the transistor in Ohmic regime, V_D = 0.08 V. Arrhenius plot of the time constant is shown in the inset.

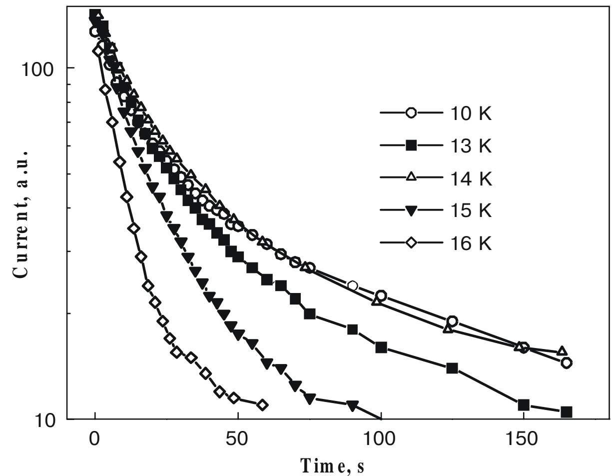

Fig. 7. Transient behaviour of the transistor in the nonlinear regime, V_D = 0.16 V.

the cases of initially empty (open) and initially filled (full) interface traps. In these measurements, firstly, the filling of traps was performed by applying the gate bias $V_G =$ = –2.6 V at temperature 23 K. Then the sample was cooled down to 10 K, drain and gate biases were applied to the terminals and the I-T characteristic was recorded during heating. It can be seen that the positive charge of traps results in an increase of the current, and when the traps are emptied, at temperatures from 16 to 18 K, the current returns back to the dependence measured at no trap filling. It should be noted that the current changes by two orders of magnitude as temperature increases by two degrees. This indicates that the effect of trapped charge on transistor operation is much greater in the subthreshold mode than in the strong inversion mode.

4. Discussion

An agreement of activation energies obtained from TSCR and transient current measurements and closeness of temperature ranges, in which these effects are observed, prove that the non-equilibrium effects of transistor operation at low temperatures is related to the charge capture in and release from the traps located in the oxide/semiconductor transition region under the gate.

The hysteresis in the output characteristics is observed at temperatures below 15 K, when the time constant of current relaxation in Ohmic mode is rather long. At such temperatures we can observe the onset of the field-assisted charge release mechanism at some value of V_D. Due to drain voltage sweep, there is no equilibrium between the voltage sweep rate and charge release. Trapped charge induces the change of the threshold voltage V_T by ΔV_T, which, in turn, is a function of time during the traps emptying. Positive charge trapped in the interface traps reduces the threshold voltage, resulting in the increase of drain current. In the linear mode the trapped charge is released very slowly, which, in turn, results in a slow variation of V_T. Since V_T changes slower than V_D, and at temperatures below 15 K is practically unchanged in the linear mode, we observe the hysteresis in the output characteristics.

At sufficiently high V_D, after reaching the pinch-off point, the transistor turns into the nonlinear mode. In this case the nonequilibrium depletion conditions exist near the drain and along the channel [14], and essential electrical fields appear in the Si/SiO_2 interface facilitating the charge emission from hole traps. Thus, the major part of the trapped charge is released under the influence of the field even at temperatures below 15 K. The increase of the gate voltage facilitates the formation of depletion layer near the drain, which also accelerates the emptying of interface traps.

The presence of a «threshold» voltage for the onset of charge emission and the slight temperature dependence of the emission process at $T < 15$ K (see Fig. 4) permit us to suggest that charge release occurs by tunneling through the potential barrier. An exact description of the emission should take into account a number of parameters related to nonuniform potential distribution along the channel of

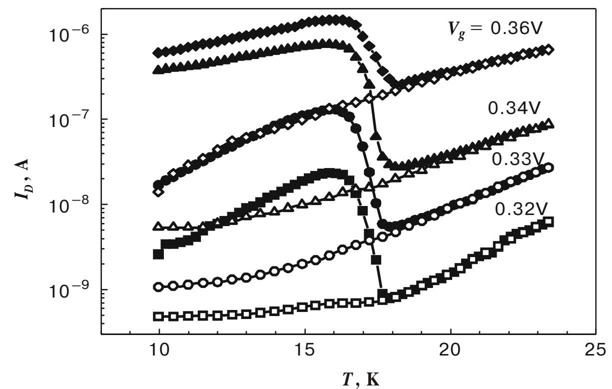

Fig. 8. Temperature dependencies of drain current of *n*-channel MOSFET for filled (full symbols) and empty (open) traps. V_D = 0.08 V, V_G is indicated near the respective curves.

the transistor and to nonuniform charge distribution in the interface, and is a fairly difficult problem. Therefore, qualitatively the processes of field charge emission from traps at the insulator-semiconductor interface were studied using the model structure, MOS capacitor.

In Fig. 9 the plots are shown illustrating the interconnection between thermally stimulated and field-induced emission of trapped charge in MOS structure. Fig. 9 (a, c, e) show thermally stimulated charge release currents. Fig. 9 (b, d) illustrate the experiments on field emission of charge at temperature 8 K. In this case charging was carried out by applying voltage of –30 V to the metal electrode at temperature 20 K, then the structure was cooled down to the temperature of measurement, and the current was recorded during the voltage sweep corresponding to transition from accumulation of the surface semiconductor layer to depletion. The studies of the field

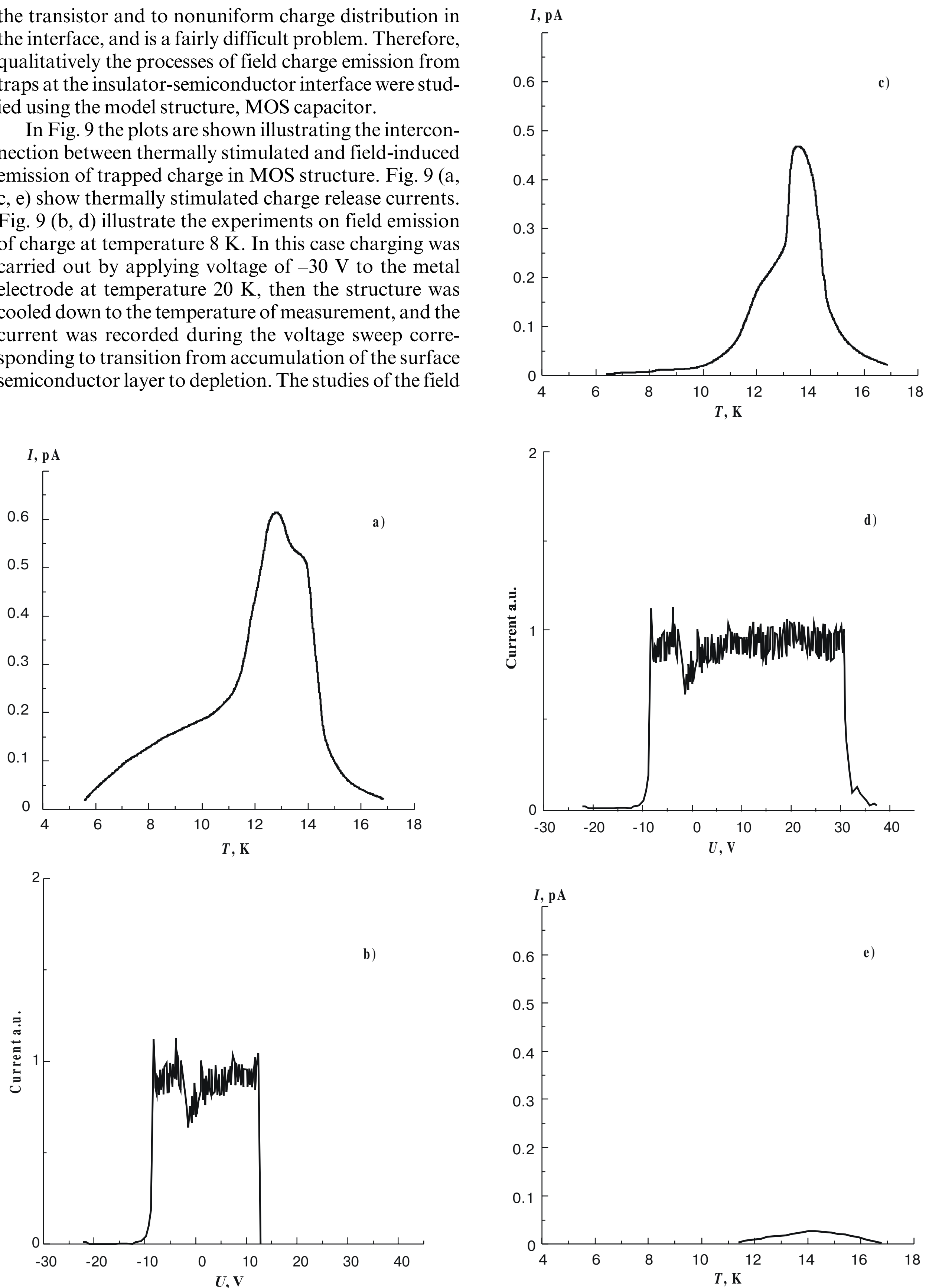

Fig. 9. Thermally stimulated charge release currents of MOS capacitor. a) – initial; c) – after field emission of half of trapped charge (b); e) – after field emission of full charge (d).

emission of charge [11] have shown that the trapped charge can be released fractionally, in parts. For example, if half of the current pulse was registered, the gate voltage was returned back to the charging value and swept again from accumulating to depleting, the second current pulse starts at the same point where the first one ends. This fact proves that the emission is controlled by the electric field. In Fig. 9 (a) TSCR current is shown after charging by $V = -30$ V. In Fig. 9 (c, e) the TSCR currents were measured after field emission of half of trapped charge (Fig. 9(b)) or of full charge (Fig. 9(d)), correspondingly. Partial field release and following TSCR recording lead to the decrease of the amplitude and to the disappearance of the low-temperature TSCR peaks. This fact evidently proves that in the field emission experiments the charge release from traps located in the Si/SiO_2 transition layer is registered.

Qualitatively the same picture is observed in transistors if the drain voltage sweep does not reach the critical value. Studies of hysteresis have shown that after trap charging the complete return to initial characteristics can be reached after several cycles of $I_D - V_D$ measurements, if the drain voltage is below the critical value. This situation is shown in Fig. 10, where a total hysteresis can be presented as a sum of two parts. Thus, we can draw the conclusion that, the same as in the case of field emission in MOS structures, the field controls charge emission from traps in the transition layer of «gate oxide-semiconductor» interface. The charge emission leads to reduction of ΔV_T with time, resulting in the decrease of extra currents (hysteresis) in the pre-kink region.

At temperatures above 15 K, the charge release takes place in the linear mode due to thermal activation and the hysteresis amplitude decreases rapidly down to a total disappearance at 17 K.

Even more convincing evidence that the determining process in the observed phenomena is the trap recharging can be obtained from the temperature dependencies of drain currents (see Fig. 8). In this case all parameters related to the control of fields in the transistor structure are fixed, i.e. all transient processes in the substrate bulk are excluded. Besides, to avoid impact ionization phenomena, drain currents were kept very low, and only temperature was changed. The strong variation of the drain current, after preliminary filling the interface hole centres, in the temperature range 16–18 K, is related exclusively to the thermally activated release of these centres.

As was shown in our previous papers [10, 11, 15], the observed thermofield effects at such low temperatures may take place with involvement of local phonons connected with defects in the transition Si-SiO_2 region. These phonons promote the carrier trapping or release at the account of carrier tunneling.

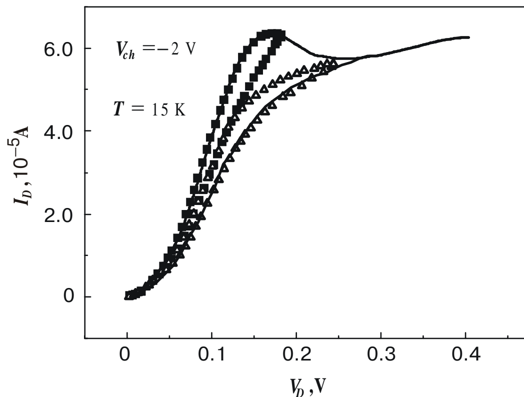

Fig. 10. Drain characteristic after trap filling (solid line) and hysteresis observed in two subsequent cycles (■ – the first cycle, △ – the second cycle).

Conclusions

During the study of low-temperature operation of *n*-channel MOSFET the non-equilibrium hysteresis effects were found, manifested as «humps» in the drain characteristics and as sharp drops of the drain current while sample heating. These effects are related to the charge state of shallow traps located in the Si/SiO_2 interface.

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