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Influence of pulse thermal annealing on photoelectrical properties of locally grown polycrystalline silicon films

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Abstract. The possibility of forming polycrystalline silicon films by pulse thermal annealing has been investigated using measurement of a photo-e.m.f., dark and light voltage-current characteristics. Investigated samples were resistors of rectangular form with the dimensions 400x40 μm^2 and had contact areas covering 100x100 μm^2. Ohmic behavior of contacts was ensured by additive diffusion of phosphorus atoms info the film under aluminium electrodes. It is shown that the samples before thermal treatment have utterly symmetrical dark and light voltage-current characteristics, which are essentially changed after samples treatment: at low applied voltages the samples resistance rises more than the order of its magnitude, and a value of a asymmetry coefficient reaches 20. Obtained results have been analyzed from the viewpoint of the model of polycrystalline film conductance taking info account intergranular barriers of the Shottky type. The conclusion is made that optimization of modes of thermal treatment regimes will enable to get rid from electroforming during fabrication of photocells based on such polycrystalline silicon film.

Keywords: polycrystalline silicon film, photoelectrical properties, *p-n* junctions.

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It is known that electroforming of the polycrystalline silicon films (PSF) by current pulses gives rise to the memory effects of anomalous photovoltage (APV) and negative capacitance [1-3]. In this case the *I-V* characteristics (IVC) of PSF, almost symmetrical in respect to the polarity of the applied voltage, become diode-like after the electroforming.

The mechanism of asymmetry induction in IVC of PSF, suggested in [4], assumes that a thermal breakdown in the current direction occurs in one of the two barrier layers at the opposite grain boundaries, namely, in the one which at a given polarity of the forming voltage is under a reverse bias.

The APV effect in PSF is of interest from the viewpoint of design of planar solar cells not requiring additional *p-n* junctions and having a high conversion factor.

However, electroforming of each separate cell by current pulses is time-consuming and is not efficient for mass production.

In this work, we studied the possibility of PSF formation by pulse thermal annealing (PTA) with the help of IR radiation using the ITO-18MV system described in [5].

The PSF under study were grown together with n-type epitaxial films (thickness 5 μm, concentration of phosphorus dopants 10^{15} cm^{-3}) on locally masked substrate KDB-10 (boron-doped silicon, 10 Ohm cm) using the technology described in [6]. Samples were the resistors of rectangular shape with linear dimensions 400×40 μm^2 and contact area 100×100 μm^2. The contact regions were additionally doped by diffusion of phosphorus atoms in order to create Ohmic contacts.

Measurements of photo-emf, dark and light IVC at illumination of 2000 lux were carried out both prior to PTA and after it, such that during PTA some samples were turned to the source of IR radiation with their front side, and the rest with the back side of the wafer. Annealing was performed at the temperature of 600 ^{O}C for 30 seconds.

Measurements on the initial samples indicated a virtually perfect symmetry of both dark and light IVC in respect to the voltage polarity (Fig. 1). The resistance of the samples at the initial part of the IVC (below the voltage ± 1 V) was ~ 2-5 MOhm, and under illumination was lower approximately by a factor of 3. Measurements in the rectifier mode have shown the presence of a small idle voltage U_{xx} (about 10 mV).

The influence of PTA on the parameters of the samples turned to the IR source with the substrate side manifested itself as an increase of the sample resistance at the initial part approximately by a factor of 2. The symmetry of IVC and the magnitude of U_{xx} remained practically unchanged (Fig. 2).

Post-PTA measurements of the samples with the back side turned to the radiator revealed an absolutely different picture (Fig. 3): dark IVC at different polarities have

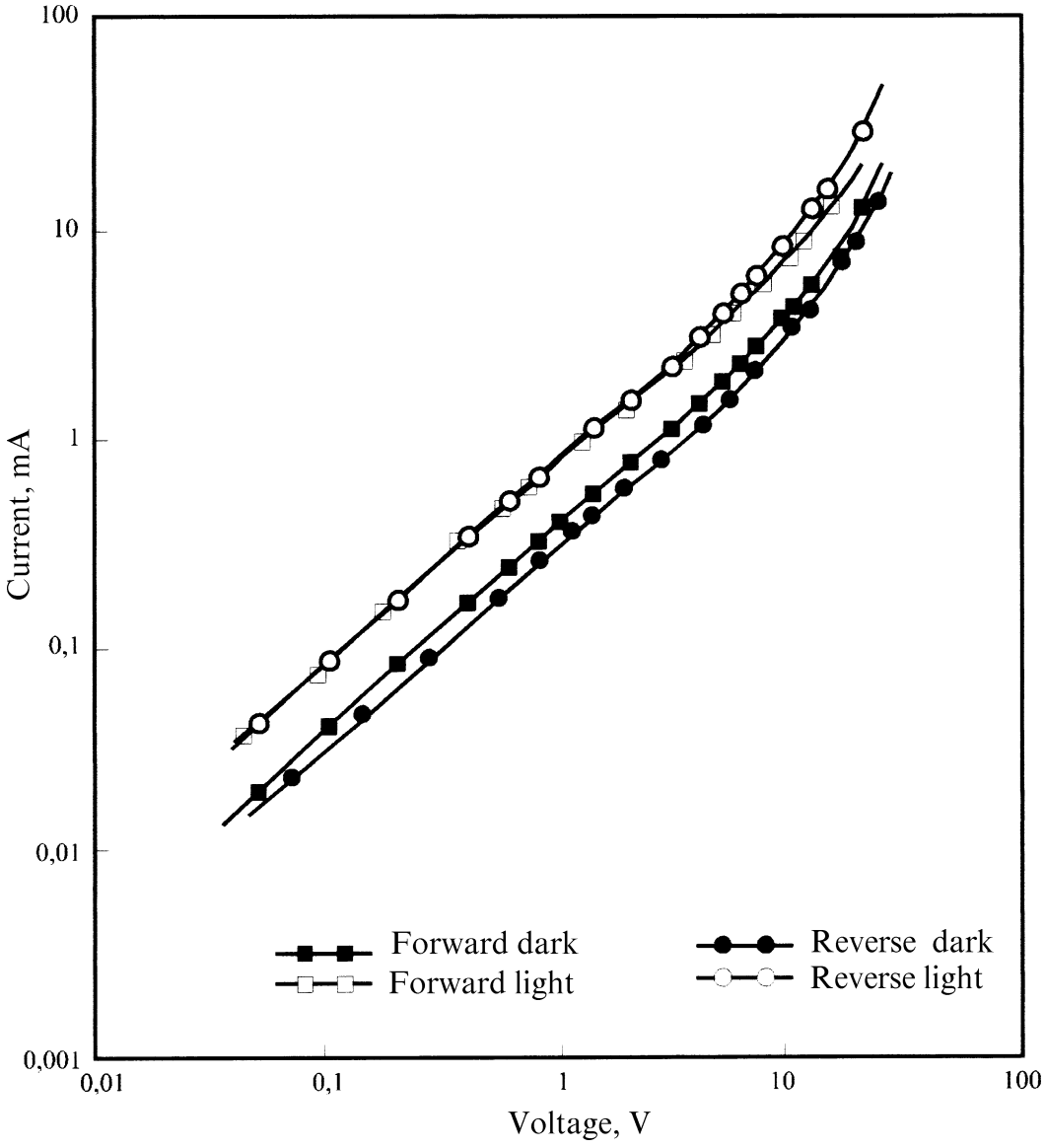

Fig. 1. I-V characteristics of the structures before pulse thermal anneling.

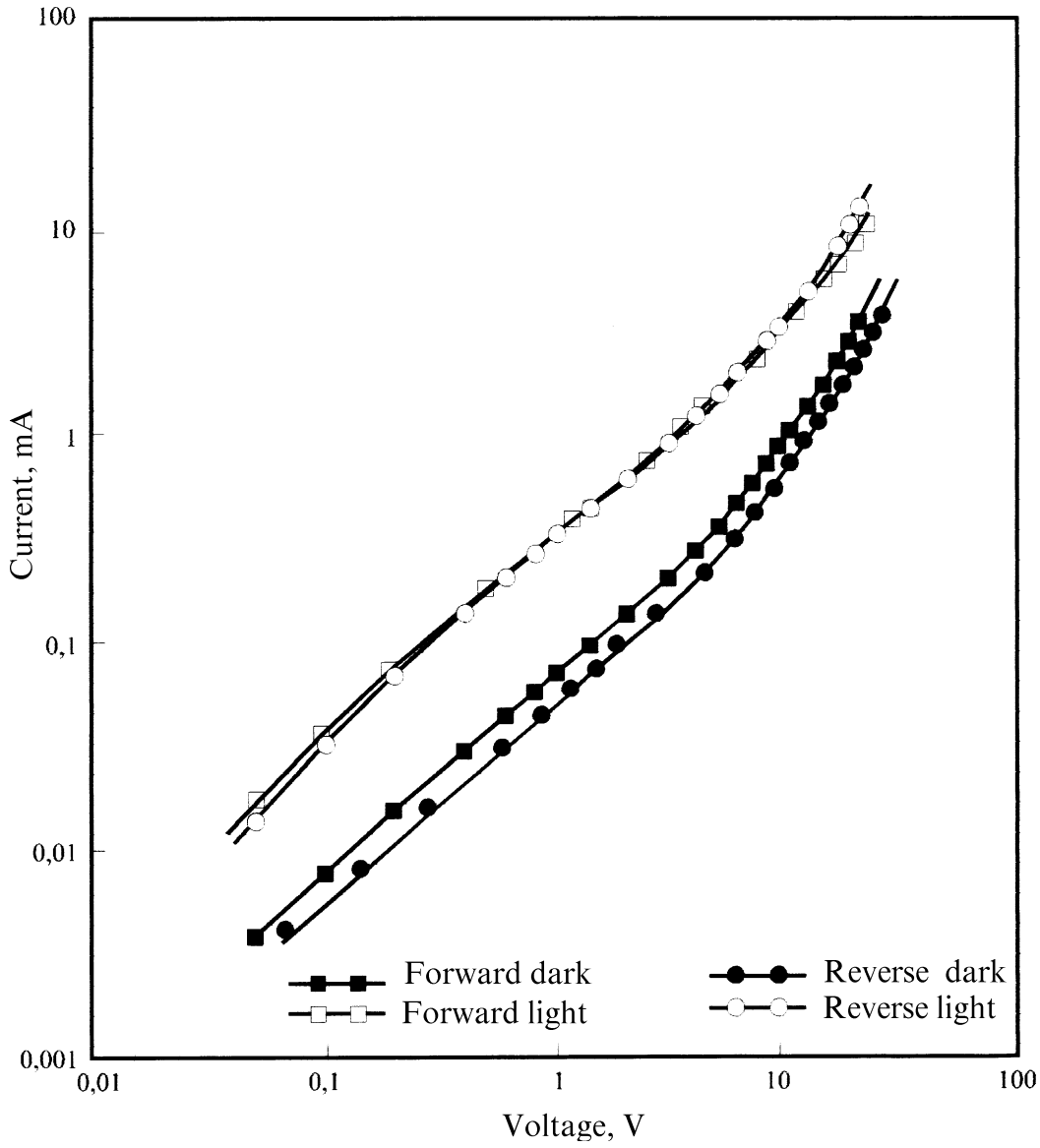

Fig. 2. I-V characteristics of the structures after pulse thermal anneling from the back side.

the coefficient of asymmetry ranging from 2 to 20; sample resistance at initial part of IVC increases at least by one order of magnitude; under illumination the sample resistance decreases by a factor of 10; the idle voltage increases up to 200 mV.

The obtained results were analyzed using the model of transport in polycrystalline films with grain boundary barriers of the Schottky type [7]. In the approximation of the diffusion theory and in assumption of the full filling of surface states at the grain boundaries, ICV of the films containing x grain boundaries in the direction of current flow is described by the equation

$$j = \frac{\mu kTN_s}{4L^2}\left(1-\frac{q^2U^2}{16\chi^2\varphi_0^2}\right)\left[1-\exp\left(-\frac{qU}{\chi kT}\right)\right]\times$$
$$\times\exp\left(-\frac{\varphi_0}{kT}+\frac{qU}{2\chi kT}-\frac{q^2U^2}{16kT\chi^2\varphi_0}\right) \qquad (1)$$

which, in dependence on the value of $\frac{qU}{\chi kT}$ can be expanded into two components:

The linear one at $\frac{qU}{\chi kT} << 1$

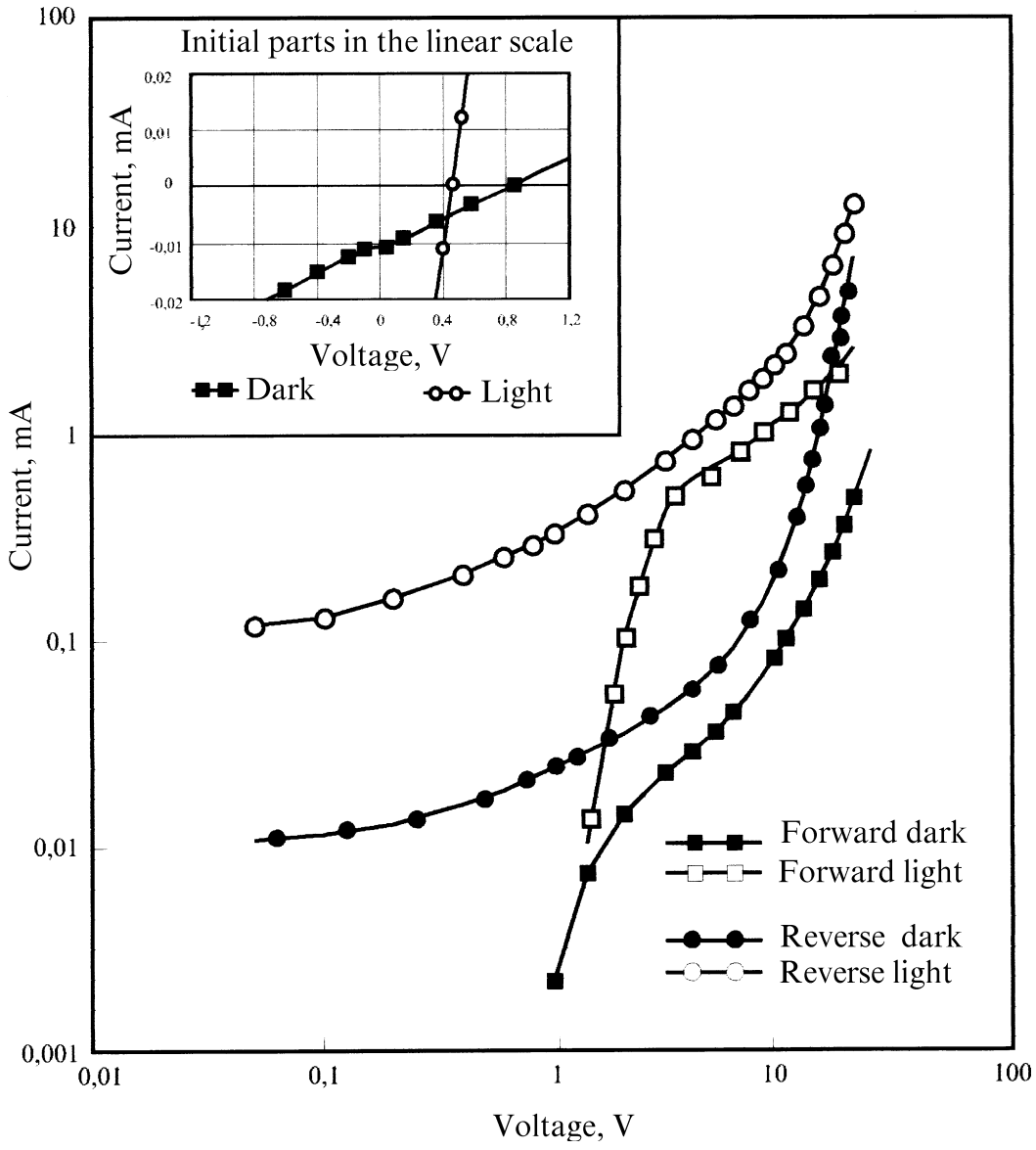

Fig. 3. I-V characteristics of the structures after pulse thermal anneling from the front side.

$$j = \frac{q\mu N_s}{4\chi L^2} U e^{-\frac{\varphi_O}{kT}}, \qquad (2)$$

and the exponential one at $\frac{qU}{\chi kT} >> 1$

$$j = \frac{\mu kTN_s}{4L^2}(1 - 4a^2U^2)Ue^{-\frac{\varphi_O}{kT}} \times \times \exp\left(\frac{q}{2\chi kT}(U - aU^2)\right), \qquad (3)$$

where m is the carrier mobility, N_s is the maximum density of states at the grain boundary, U is the applied voltage, $\varphi_0 = \frac{\pi q^2 N_s^2}{2\varepsilon\varepsilon_O N_D}$ is the height of the potential barrier at U=0, $\varepsilon\varepsilon_O$ is the dielectric constant of silicon, $L^2 = \frac{\varepsilon\varepsilon_o kT}{4\pi q^2 N_D}$ is the Debye length, N_D is the donor concentration in the semiconductor.

The results of calculations of the electrical parame-

ters of the samples not subjected to thermal annealing are presented in Table 1, and the parameters of the samples after PTA with back and front side turned to the radiator are presented in Tables 2 and 3, respectively.

For the initial sample not subjected to PTA, the electrical parameters calculated at different bias polarities have practically equal magnitudes, which could be expected taking into account the symmetry of the characteristics. The illumination results in an increase of the potential barrier height at the grain boundaries, of the degree of filling of the surface states and of the free carrier concentration within the grain.

In the equilibrium conditions, the barrier height and width of the depletion layer are the same on both sides of the grain. The illumination of the sample results in the electron-hole pair generation both near the grain boundaries and in the grain bulk. The electrons generated near the grain boundaries are captured in the interface states and recombine with the holes, i.e. there is no the change of the barrier height. The total photo-emf in this case is less than 10 mV, which was observed in the experiment.

When the voltage is applied, the barrier at the forward-biased side of the grain is lowered, and its width is reduced, resulting in an additional electron capture to the interface states of the forward-biased barrier, which causes an increase of its height. The barrier at the opposite side of the grain is increased, and the depletion layer becomes wider. Under the illumination, this process in the forward-biased barrier will be more pronounced, because the photogenerated electrons move to the forward-biased barrier in the external field, and, being captured in the interface states, increase its height. This results in the increase of the voltage of transition to the exponential section of IVC by a factor of 1.5-2. The photoholes moving to the opposite side of the grain recombine with electrons at the interface states, lowering the height of reverse-biased barrier and increasing the current through the structure. If the voltage of the opposite polarity is applied, the forward- and reverse-biased barriers are exchanged, but the total behavior remains the same.

If PTA is performed from the back side, the silicon wafer absorbs all radiation, and the parameters of PSF are affected by the temperature regime of PTA only.

It can be seen from the comparison of Tables 1 and 2 that PTA from the back side resulted in the reduction of the carrier concentration in the grain bulk n_g and of filling of interface states N_S, and, as a result, the intergrain barrier height increases and the total current across the sample decreases. The symmetry of parameters in respect to the polarity of external bias and the effect of the sample illumination remains unchanged as compared to the initial sample.

It should be noted that the results presented in the tables are the average values for all grains. However, the grains in PSF vary significantly both by their size and by the crystallographic orientation. Therefore, the difference of the barrier heights at opposite sides of the grain may

Table 1. Electrical parameters of polysilicon structures before pulse thermal anneling.

REGIME/ PARAMETER	REVERSE BIAS		FORWARD BIAS	
	DARK	LIGHT	DARK	LIGHT
φ_0, eV	0.048	0.077	0.052	0.075
N_s, cm^{-2}	$5.2.10^9$	$1.25.10^9$	6.10^9	$1.2.10^9$
n_g, cm^{-3}	$1.3.10^{14}$	$4.9.10^{14}$	$1.7.10^{14}$	$4.6.10^{14}$

Table 2. Electrical parameters of polysilicon structures after pulse thermal anneling from the back side.

REGIME/ PARAMETER	REVERSE BIAS		FORWARD BIAS	
	DARK	LIGHT	DARK	LIGHT
φ_0, eV	0.054	0.063	0.06	0.069
N_s, cm^{-2}	$4.7.10^9$	$8.9.10^9$	$5.3.10^9$	$9.7.10^9$
n_g, cm^{-3}	$9.7.10^{13}$	$2.8.10^{13}$	$1.1.10^{14}$	$3.2.10^{14}$

Table 3. Electrical parameters of polysilicon structures after pulse thermal anneling from the front side.

REGIME/ PARAMETER	REVERSE BIAS	
	DARK	LIGHT
$\varphi_{0,}$ eV	0.22	0.074
N_s, cm^{-2}	$2.3.10^{10}$	$7.5.10^{9}$
$n_{g,}$ cm^{-3}	$5.6.10^{14}$	$6.0.10^{14}$

be much greater than the mean values presented in the table.

Also, it should be taken into account that the conductivity in PSF actually takes place not only through the barriers in the grain boundaries, but in the intergrain sub-layers parallel to the current direction. In this case, the number of grains taking part in the conductance will be determined by their size and the depletion layer width. Small grains can be fully covered by the depletion layer and will not be able to contribute to the conduction process.

If PTA is performed from the front side, an intense photoabsorption takes place in PSF, which results, as seen from Fig. 3, in the essential transformation of IVC of the sample in comparison to the initial one. The voltage of the transition to the exponential part of IVC becomes lower, and the sublinear part is practically absent. Because of this, the calculation of electrophysical parameters (Table 3) was performed using only the reverse branch of IVC which included all considered parts.

It is seen from the data presented in Table 3 that the barrier height increases by the factor of 5 after PTA, and the free carrier concentration in the grain bulk and the concentration of filled interface states in the grain boundaries also rise by the factor of 4. Moreover, the appearance of the idle voltage of ~ 400 mV and reduction of the barrier height during sample illumination should be noted.

These results can be explained by the influence of an internal electric field due to difference of potential barriers at opposite sides of the grain, the effect of which becomes especially essential at the high level of illumination during the PTA.

The electric field leads to the spatial separation of carriers generated during that PTA. As a result, the barrier at one side of the grain (initially the lower one) increases due to electron capture at the empty interface states, and the height of the opposite barrier reduces due to recombination with photoholes. Therefore, after the pulse thermal annealing from the front side of the wafer we get a diode-like asymmetrical structure with some excess concentration of minority carriers, i.e., of holes avoiding recombination, which determine the shift of IVC. Under illumination, IVC of such samples show a higher reverse current, and the potential barrier height reduces due to the recombination of photoholes with electrons at the interface states. The barrier at the opposite side of the grain in this case is so small that it is completely compensated by the external electric field, and, therefore, the capture of photoelectrons in the interface states is negligible. This is also confirmed by the absence of the sub-linear part in the forward branch of IVC of the sample subjected to PTA from the front side.

The investigations show that further optimization of the conditions of pulse thermal annealing of polycrystalline silicon films will make it possible to substitute the electroforming by current pulses, which is performed to obtain APV elements, by the batch treatment using the effect of intense irradiation in the IR range.

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