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Optimal solution in producing 32-nm CMOS technology transistor with desired leakage current

H.A. Elgomati[1], I. Ahmad[2], F. Salehuddin[2,5], F.A. Hamid[2], A. Zaharim[3], B.Y. Majlis[1], P.R. Apte[4]
[1]Institute of Microengineering and Nanoelectronic University Kebangsaan Malaysia (UKM),
43600 Bangi, Selangor, Malaysia,
E-mail: hus_7119@yahoo.com; burhan@eng.ukm.my;
[2]College of Engineering University Tenaga National (UNITEN),
43009 Kajang, Selangor, Malaysia,
E-mail: aibrahim@uniten.edu.my; fauziyah@utem.edu.my; fazrena@uniten.edu.my;
[3]Faculty of Engineering and Built Environment University Kebangsaan Malaysia (UKM),
43600 Bangi, Selangor, Malaysia,
E-mail: azami.zaharim@gmail.com;
[4]Indian Institute of Technology (IIT), Bombay, Powai, Mumbai-400076, India,
E-mail: apte@ee.iitb.ac.in;
[5]University Technical Malaysia Melaka (UTeM),
Durian Tunggal, Melaka, Malaysia

Abstract. The objective of this paper is to optimize the process parameters of 32-nm CMOS process to get minimum leakage current. Four process parameters were chosen, namely: (i) source-drain implantation, (ii) source-drain compensation implantation, (iii) halo implantation time, and (iv) silicide annealing time. The Taguchi method technique was used to design the experiment. Two noise factors were used that consist of four measurements for each row of experiment in the L_9 array, thus leading to a set of experiments consisting of 36 runs. The simulator of ATHENA and ATLAS were used for MOSFET fabrication process and electrical characterization, respectively. The results clearly show that the compensation implantation (46%) has the most dominant impact on the resulting leakage current in NMOS device, whereas source-drain (S/D) implantation was the second ranking factor (35%). The percent effects on signal-to-noise ratio (SNR) of silicide annealing temperature and halo implantation are much lower being 12% and 7%, respectively. For the PMOS device, halo implantation was defined as an adjustment factor because of its minimal effect on SNR and highest on the means (43%). Halo implantation doping as the optimum solution for fabricating the 32-nm NMOS transistor is 2.38×10^{13} atom/cm^3. As conclusion, this experiment proves that the Taguchi analysis can be effectively used in finding the optimum solution in producing 32-nm CMOS transistor with acceptable leakage current, well within International Technology Roadmap for Semiconductor (ITRS) prediction.

Keywords: 32-nm device, halo, compensation implant, leakage current, Taguchi method.

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1. Introduction

Moore's Law-driven technology scaling has improved VLSI performance by five orders of magnitude in the last four decades. As advanced technologies continue the pursuit of Moore's Law, a variety of challenges will need to be overcome [1]. Moreover, the increasing statistical variation in the process parameters has emerged as a serious problem in the nano-scaled circuit design and can cause significant increase in the transistor leakage current [2, 3]. One of the main complications is to control the gate leakage current of the transistor [4]. Designing with the worst case leakage current may cause excessive guard-banding, resulting in lower performance [2, 3]. Therefore, accurate estimation of the total leakage current considering the effect of random variations in the process parameters is extremely important for designing CMOS circuits in the nano-material regime. Various

leakage mechanisms contribute to the total leakage in device [4]. Sub-threshold leakage, gate leakage and reverse biased drain substrate junction band-to-band-tunnelling leakage are the major mechanisms that contribute to the total leakage current [5, 6]. Hence, each component depends differently on the transistor geometry such as gate length, source-drain extension length, oxide thickness, junction depth, width, doping profile (channel doping and "halo" doping concentration, flat band voltage and supply voltage) [5, 6]. Statistical variation in each of these parameters results in large variation in each of the leakage components, thereby, causing significant increase in the nominal leakage. Thus, there is a need for detailed and systematic analyses of the relationships between process design parameters and overall design function and leakage current characteristic and to use the resulting data in behavioral modeling and robust design. Therefore, the Taguchi method that is robust design method of experiment is required to optimize the process parameters variation in order to fabricate 32-nm CMOS device with a minimum leakage current. Taguchi experimental design and statistical process-controlling methods provide efficient means for conducting performance variability reduction and parametric sensitivity analyses and are used for off-line parametric optimization control and high-performance design [7]. The objective is to identify the parameters or factors most influential in determining a performance metric and to compute the settings of the parameters that yield both an acceptable performance metric and minimize the influence of parametric variations. In other words, sensitivity to product-design parameter variation is reduced by choosing levels of controllable parameters that maximize design insensitivity to the variance of a set of noise factors denoting sources. Experimental data is generated using orthogonal arrays. Orthogonal arrays simplify factorial sampling strategies, making it computationally feasible to evaluate directly the effect of different noise factors on performance variability. Orthogonal arrays also standardize factorial sampling strategies in a manner that yields consistent data for estimating the contribution of individual parameters to overall design robustness. Taguchi performance-variability reduction and parametric sensitivity analyses introduce design-for-manufacturing into behavioral modeling. Performing off-line control modeling and simulation before actual fabrication is becoming an important aspect for fabrication process of nano-scaled CMOS devices-design optimization due to high costs of fabrication and difficulties of controlling the inherent stochastic nature of fabrication processes. The emphasis is on maximizing the insensitivity of the design to a known set of parametric variations, rather than on minimizing the parametric variations themselves.

In this paper, four parameters, namely: halo implantation, source drain implantation, source drain compensation implantation and silicide annealing temperature were selected and optimized in order to obtain the robust recipe for minimizing the leakage current in the 32-nm MOSFET device. The Taguchi orthogonal L_9 array method technique was used in the experiment. The medium experiment was technology computer aided design (TCAD) of ATHENA and ATLAS for device fabrication processes and device electrical characterization, respectively. The adoption and verification of the robust recipe of 32-nm MOSFET for a minimum leakage current were introduced.

2. Experiment description

The substrate used for experiment was silicon of p-type with ⟨100⟩ orientation. Most of the process steps for 32-nm CMOS process were similar to those in [8, 9]. An oxidation layer, the top layer obtained using dry oxygen was prepared at the temperature 970 ºC for 20 min. P-well implantation process was done using this oxide layer as a mask. It was made using boron as dopant with the dose close to 3.75×10^{12} ions/cm^2 and the implantation energy of 100 eV. The ion gun was 7º tilted. Then, the silicon wafer undergone the annealing process. This process lasted for 30 min in nitrogen and then in dry oxygen for 36 min in order to ensure that boron atoms being spread properly in the wafer. The masking oxide was then etched. The following step was to produce shallow trench isolator (STI) of 130-Å thickness [10]. In order to form the STI layer, the wafer was oxidized in dry oxygen for 25 min at 900 ºC. Then, a 1500-Å nitride layer was deposited on the top of oxide layer by applying low pressure chemical vapour deposition process (LPCVD) followed by photoresist deposition with the thickness 1.0 μm. Then, the photoresist and nitride were etched using reactive ion etching process (RIE) at the top of STI area. The trench depth of 3241 Å was achieved in 0.36-min process. Thereafter, a sacrificial oxide layer was grown and then etched, which was followed by a sacrificial nitride layer. The trench then completed. To introduce a process noise (N1), in a second run of the device fabrication process, the diffusion temperature was increased up to 901 ºC. The following process was to grow the gate oxide. To reach it, the silicon wafer was oxidized with dry oxygen at 825 ºC at 1.0 atm for a short time. The short time is needed to ensure a very thin layer, and no more than 1.1 nm of oxide thickness was grown. Then, the next step was to implant phosphorus and boron difluoride (BF_2) at both N- and P-well active areas, respectively, in order to adjust the threshold voltage V_{th} value. The dosages for phosphorus and boron were 1.75×10^{11} and 3.5×10^{11} ions/cm^2, respectively. The energy for both implantations was 5 eV, and the ion beam was tilted at 7º. Then, polysilicon should be deposited on the top of the wafer and etched accordingly to produce the gate contact point as desired. Halo implantation then took place on both sides, P- and N-well active areas, indium with the dose 6×10^{12} ions/cm^2 was embedded at the energy 120 keV. The beam was 30º tilted when implanting. The dosage was varied in order to get the

optimum value as shown in Table 1. Then, the nitride layer was deposited on the top of polysilicon gate and immediately etched to expose the top surface of silicon layer. Then spacers were formed at each of the polysilicon sides, namely: source and drain regions, respectively. The silicon nitride layer of 0.0423-μm thickness was deposited [11]. Then it was etched away for the same thickness. Due to nature of the substrate surface with gate, side-wall spacers were created as the thickness at the gate sides was 0.0867 μm. Side-wall spacers were used as a mask for source and drain implantation [12]. Then, there were source-drain implantations for both PMOS and NMOS. For PMOS, prior to implantation of source and drain, photoresist was deposited and etched for source and drain areas, firstly boron with dose of 1.0×10^{14} ions/cm^2, 12 keV implantation energy and 7º was tilted, followed by phosphorous with dose of 1.5×10^{12} ions/cm^2, 12 keV implantation energy and also was 7º tilted. For NMOS, the first implantation was arsenic of 5.1×10^{13} ions/cm^2, at 15 keV of energy then followed by 7.65×10^{11} ions/cm^2. The following process was to diffuse the dopants at 900 °C for 10 min. Thereafter, depositing an oxide mask on the top of polysilicon gate in order to form a silicide structure on both PMOS and NMOS. The cobalt silicide layer of 0.0867-μm thickness was then deposited on the top of substrate and then annealed by rapid thermal annealing process in nitrogen environment. It was made at 1100 °C. However, the temperature was varied as in Table 1 in order to obtain three different thicknesses and ion distribution for optimization. Afterwards, the unwanted area of cobalt was etched away. The introduction of the second noise happens at the next step, where the annealing of the structure for 6 s at the temperature 910 ºC in nitrogen environment at 1 atm. The noise (N2) was introduced by reducing the anneal temperature to 909 ºC. This annealing process was to deepen spread the cobalt atoms into polysilicon. The next process was the development of 0.3 μm borophosphosilicate glass (BPSG) layer [13]. This layer acts as pre-metal dielectric (PMD). PMD contains silicon dioxide that was doped with boron and phosphorus. After BPSG deposition, the wafer undergone 20-min annealing at the temperature 850 °C. The next process was compensation implantation with the dose 2.5×10^{13} ions/cm^2, 60-eV implantation energy, and the beam was 7º tilted for PMOS and 2.5×10^{13} ions/cm^2, 50-eV implantation energy, and the beam was 7º tilted for NMOS [14]. Then, it was followed by aluminium contact deposition. Then, the wafer was annealed for 20 min at 850 ºC. Next, the aluminium layer was deposited on the top of structure and then etched accordingly to form metal contacts for source and drain. Thus, production of the transistor was completed. Then, the transistor has undergone electrical characteristic measurements in order to find the leakage current. Figs 1 and 3 show the completed NMOS and PMOS transistors, while Figs 2 and 4 show the doping profiles for the same structures.

3. Taguchi method using L_9 orthogonal array

In this work, the $L_9(3^4)$ orthogonal array that has 9 experiments was used. We used four process parameters, namely: source drain implantation, compensation source drain implantation, halo implantation and silicide annealing time. The values of these four process parameters at the different levels are listed in Table 1. The experimental layout for the process parameters using the $L_9(3^4)$ orthogonal array is shown in Table 2.

Two noise factors will create four measurements for each row of experiment in the L_9 array, thus leading to a set of experiments consisting of 36 runs. A set of four measurements for each row of L_9 orthogonal array is the minimum number of results needed for our project using the Taguchi analysis.

Table 1. Process parameters and their levels.

Device	Symbol	Process parameter	Unit	Level 1	Level 2	Level 3
NMOS	A	halo implantation	atom/cm^3	1.285×10^{13}	1.28×10^{13}	1.27×10^{13}
	B	S/D implantation	atom/cm^3	5.1×10^{13}	5.0×10^{13}	4.9×10^{13}
	C	compensation implantation	atom/cm^3	3.8×10^{13}	3.7×10^{13}	3.6×10^{13}
	D	silicide annealing temperature	°C	890	900	910
PMOS	A	halo implantation	atom/cm^3	2.35×10^{13}	2.38×10^{13}	2.40×10^{13}
	B	S/D implantation	atom/cm^3	6.55×10^{11}	6.60×10^{11}	6.65×10^{11}
	C	compensation implantation	atom/cm^3	2.9×10^{13}	3.0×10^{13}	3.1×10^{13}
	D	silicide annealing temperature	°C	900	910	950

Table 2. Experimental layout using $L_9(3^4)$ orthogonal array.

Exp. No.	Process parameter level			
	A halo implan-tation	B S/D implan-tation	C compensa-tion implan-tation	D silicide annealing tempera-ture
1	1	1	1	1
2	1	2	2	2
3	1	3	3	3
4	2	1	2	3
5	2	2	3	1
6	2	3	1	2
7	3	1	3	2
8	3	2	1	3
9	3	3	2	1

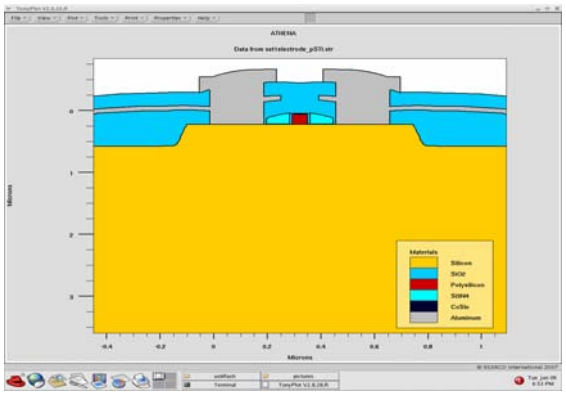

Fig. 1. Completed NMOS transistor.

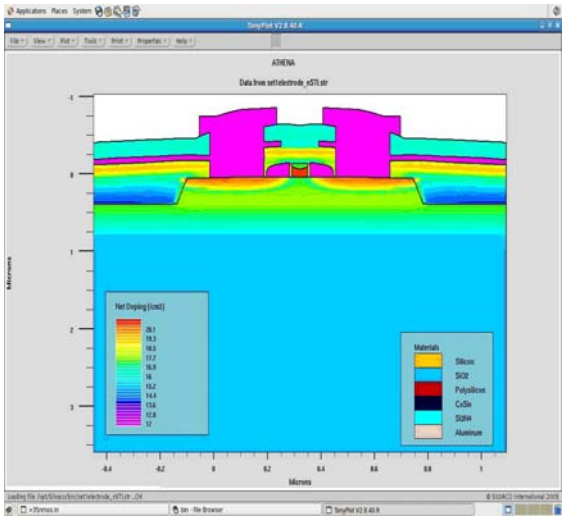

Fig. 2. The doping profile of the NMOS transistor.

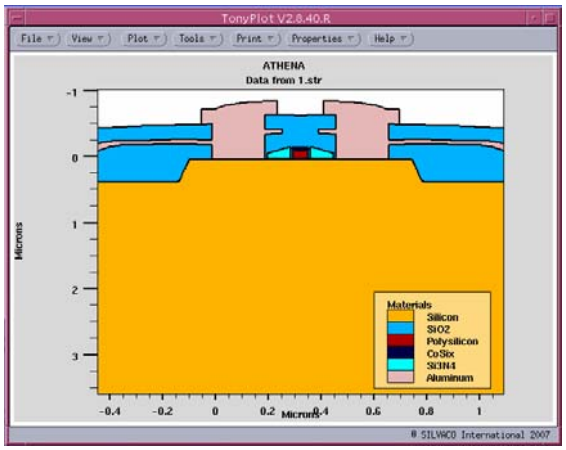

Fig. 3. Completed PMOS transistor.

4. Results and discussion

The results concerning the leakage current (I_{leak}) were analyzed and processed with the Taguchi method for boron doping to get the optimal design. The optimized results from the Taguchi method were simulated in order to verify the predicted optimal design.

4.1. Analysis for 32-nm NMOS and PMOS device

The experimental results as to the leakage currents for NMOS and PMOS devices are shown in Tables 3 and 4, respectively.

The leakage current of the 32-nm devices belongs to the smaller-the-best quality characteristics. The SNR η can be expressed as:

$$\eta = -10\log_{10}\left[\frac{1}{n}\sum\left(Y_1^2 + Y_2^2 + ... + Y_n^2\right)\right]. \qquad (1)$$

While μ is mean and σ is variance. By applying Eq. (1), η for each device has been calculated and given in Table 5.

The effect of each process parameter on SNR at different levels can be separated out, because the experimental design is orthogonal. The SNR values for each level of the process parameters are summarized in Table 6. In addition, the total mean of SNR for these 9 experiments has been also calculated and listed in Table 6.

Table 3. I_{leak} values for NMOS device.

Exp. No.	Leakage current (μA/μm)			
	$I_{leak}1$	$I_{leak}2$	$I_{leak}3$	$I_{leak}4$
1	0.157660	0.114130	0.115765	0.114131
2	0.111451	0.109858	0.111449	0.109850
3	0.107139	0.105581	0.107157	0.105580
4	0.112180	0.112181	0.113780	0.112179
5	0.109490	0.107938	0.109520	0.107962
6	0.111520	0.110710	0.112376	0.110732
7	0.111930	0.110376	0.112180	0.110400
8	0.114789	0.113036	0.115893	0.113059
9	0.110505	0.108918	0.111792	0.108939

Table 4. I_{leak} values for PMOS device.

Exp. No.	Leakage current (μA/μm)			
	$I_{leak}1$	$I_{leak}2$	$I_{leak}3$	$I_{leak}4$
1	0.10813	0.15857	0.1212	0.11113
2	0.11286	0.11351	0.1132	0.10589
3	0.10413	0.10614	0.1328	0.10456
4	0.11121	0.11441	0.1159	0.11124
5	0.10787	0.10913	0.2017	0.10879
6	0.11017	0.11025	0.1957	0.11081
7	0.11056	0.11200	0.1122	0.11052
8	0.11206	0.11404	0.1151	0.11311
9	0.10320	0.11791	0.1318	0.10881

Table 5. SNR for I_{leak}.

Exp. No.	SNR (dB)	
	NMOS	PMOS
1	137.94	137.97
2	139.12	139.06
3	139.46	138.97
4	138.97	138.92
5	139.27	137.21
6	139.07	137.28
7	139.08	139.07
8	138.85	138.89
9	139.17	138.72

Table 6. SNR for the leakage current.

Device	Symbol	Process parameter	SNR (smaller-the-best)			Total mean SNR	max - min
			Level 1	Level 2	Level 3		
NMOS	A	halo implantation	138.84	139.10	139.03		0.26
	B	S/D implantation	138.66	139.08	139.23		0.57
	C	compensation implantation	138.62	139.09	139.27	138.99	0.65
	D	silicide annealing temperature	138.79	139.09	139.09		0.21
PMOS	A	halo implantation	138.67	137.80	138.89		1.09
	B	S/D implantation	138.65	138.39	138.32		0.33
	C	compensation implantation	138.05	138.90	138.42	138.45	0.85
	D	silicide annealing temperature	137.96	138.47	138.93		0.97

Figs 5 and 6 show SNR graphs of NMOS and PMOS devices, respectively, where the dashed line is the value of the total mean of SNR. Basically, the larger SNR, the quality characteristic for the leakage current is better.

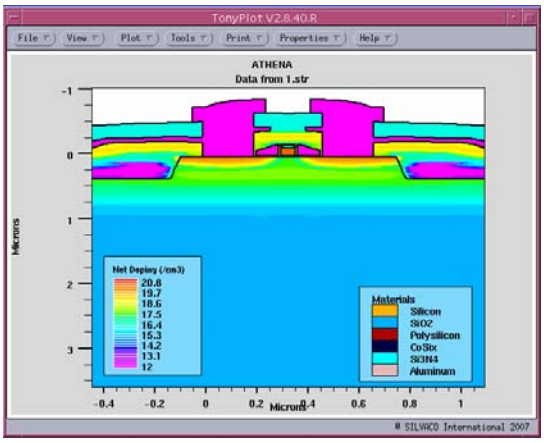

Fig. 4. The doping profile of the PMOS transistor.

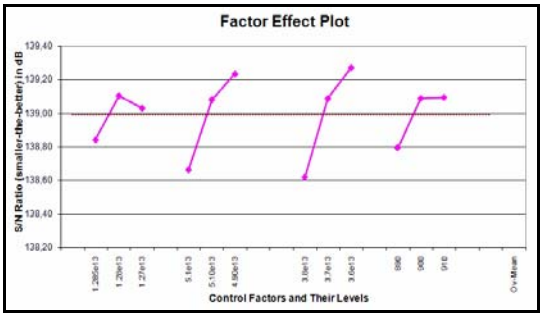

Fig. 5. Signal-to-noise ratio graph for leakage current in NMOS device.

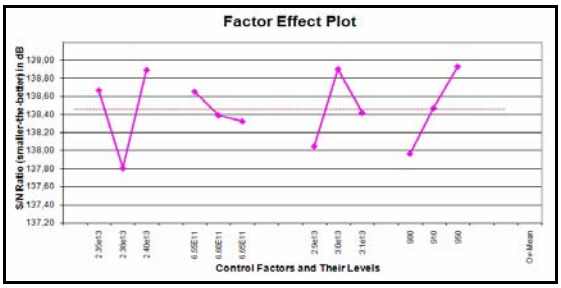

Fig. 6. Signal-to-noise ratio graph for leakage current in PMOS device.

4.2. Analysis of variance (ANOVA) for 32-nm NMOS and PMOS devices

The priority of the process parameters with respect to I_{leak} was investigated to determine more accurately the optimum combinations of the process parameters. The result of ANOVA for the NMOS device is presented in Table 7. The percent factor effect on SNR indicates the priority of a factor (process parameter) to reduce variation. For a factor with a high percent contribution will have a great influence on the performance.

The results clearly show that the compensation implantation (46%) has the most dominant impact on the resulting leakage current in NMOS device, whereas S/D implantation was the second ranking factor (35%). The percent effects on SNR of silicide annealing temperature and halo implantation are much lower, being 12% and 7%, respectively.

The optimized factors for NMOS device were been suggested using the Taguchi method are shown in Table 8. For the NMOS device, compensation implantation was defined as an adjustment factor because of its minimal effect on SNR but highest on the means (46%). Several simulations have been made with different values of compensation implantation to get the gate leakage current (I_{leak}) at a nominal value or target value. The value of compensation implantation was

adjusted within 3.8×10^{13} to 3.6×10^{13} atoms/cm^3 until the value of gate leakage current (I_{leak}) becomes closer to 0.15 μA/μm. By doing the value sweep, the compensation implantation doping as the optimum solution for fabricating a 32-nm NMOS transistor is 3.67×10^{13} atom/cm^3.

Table 7. Result of ANOVA for NMOS device.

Symbol	Process parameter	Degree of freedom	Sum of square	Mean square	Factor effect on SNR(%)
A	halo implantation	2	0	0	7
B	S/D implantation	2	1	0	35
C	compensation implantation	2	1	0	46
D	silicide annealing temperature	2	0	0	12

Table 8. The optimized factors for NMOS device.

Symbol	Process parameter	Unit	Best value
A	halo implantation	atom/cm^3	1.28×10^{13}
B	S/D implantation	atom/cm^3	4.90×10^{13}
C	compensation implantation	atom/cm^3	3.60×10^{13}
D	silicide annealing temperature	°C	910

Table 9. Result of ANOVA for PMOS device.

Symbol	Process parameter	Degree of freedom	Sum of square	Mean square	Factor effect on SNR(%)
A	halo implantation	2	2	1	43
B	S/D implantation	2	0	0	4
C	compensation implantation	2	1	1	24
D	silicide annealing temperature	2	1	1	30

The result of ANOVA for the PMOS device is presented in Table 9. The results clearly show that the halo implantation (43%) has the most dominant impact on the resulting leakage current in PMOS device, whereas silicide annealing temperature was the second ranking factor (30%). The percent effect on SNR of compensation implantation and S/D implantation are much lower, being 24% and 4%, respectively.

Table 10. The optimized factors for PMOS device.

Symbol	Process parameter	Unit	Best value
A	halo implantation	atom/cm^3	2.40×10^{13}
B	S/D implantation	atom/cm^3	6.60×10^{11}
C	compensation implantation	atom/cm^3	3.00×10^{13}
D	silicide annealing temperature	°C	950

Table 11. Results of the confirmation experiment.

Device	Symbol	Process parameter	Unit	Best value
NMOS	A	halo implantation	atom/cm^3	1.28×10^{13}
	B	S/D implantation (as an adjustment factor)	atom/cm^3	4.90×10^{11}
	C	compensation implantation	°C	3.67×10^{13}
	D	silicide anneal temperature	°C	910
PMOS	A	halo implantation	atom/cm^3	2.38×10^{13}
	B	S/D implantation	atom/cm^3	6.60×10^{11}
	C	compensation implantation (as an adjustment factor)	°C	3.0×10^{13}
	D	silicide annealing temperature	°C	950

Table 12. Results of further runs of confirmation experiment with added noises.

Device	V_{th} (n1,n1)	V_{th} (n1,n2)	V_{th} (n2,n1)	V_{th} (n2,n2)
NMOS	0.142	0.145	0.143	0.144
PMOS	0.143	0.152	0.151	0.148

The optimized factors for PMOS device which were suggested using the Taguchi method are shown in Table 10. For the PMOS device, halo implantation was defined as an adjustment factor because of its minimal effect on SNR and highest on the means (43%). Several simulations have been made with different values of halo implantation to get the gate leakage current (I_{leak}) at a nominal value or target value. The value of halo implantation was adjusted within 2.4×10^{13} to 2.35×10^{13} atom/cm^3 until the value of gate leakage current (I_{leak}) becomes closer to 0.15 μA/μm. By doing the value sweep, the halo implantation doping as the optimum solution for fabricating a 32-nm NMOS transistor is 2.38×10^{13} atom/cm^3 (Table 11).

From the above results of further runs of confirmation experiment with added noises as shown in Table 12 for NMOS, the mean is 0.1435 μA/μm with SNR equal to 26. While for PMOS, the mean is 0.1485 μA/μm with SNR close to 29. The values are well corresponded within the target set by ITRS [16].

5. Conclusion

Both 32-nm NMOS and PMOS are getting different effects from the four factors in their fabrication. For NMOS, compensation implantation was defined as an adjustment factor because of its minimal effect on SNR but highest on the means. While for PMOS, halo implantation was defined as an adjustment factor. By varying these factors while having the others fixed, we are able to find the optimum fabrication solution that will result in an operating transistor. This experiment proves that the Taguchi analysis can be effectively used in finding the optimum solution for production of the 32-nm CMOS transistor with an acceptable leakage current, well within International Technology Roadmap for Semiconductor (ITRS) prediction.

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