DEVELOPMENT OF NEW ELEMENTS OF AUTOMATED CONTROL SYSTEMS LINEAR ACCELERATOR

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For monitoring systems and control of linear electron accelerators have been designed, manufactured and introduced new elements instead of physically and morally outdated. This family of analog-to-digital converters ADC 01, ADC-02 ADC-03, ADC-05 ADC-06 have been developed in cooperation with the KNURE, and synchronizer for linear accelerator LUE-60M, designed forces of employees the research complex "ACCELERATOR" KIPT. Purpose, characteristics, technical description, block diagrams of family of analog-to-digital converters ADC01…ADC06 and of synchronizer of linear accelerator LUE-60M is presented in a report. These devices are developed on a new element base and inculcated in automated control systems of linear accelerators.

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1. ANALOG-DIGITAL CONVERTER ADC-01

Analog-digital converter ADC-01 (hereinafter referred device) designed for synchronous digitizing of four analog signals in the 8-bit binary code and write data to computer memory. The device is using a computer via the PCI. The block diagram of the converter is shown in Fig. 1.

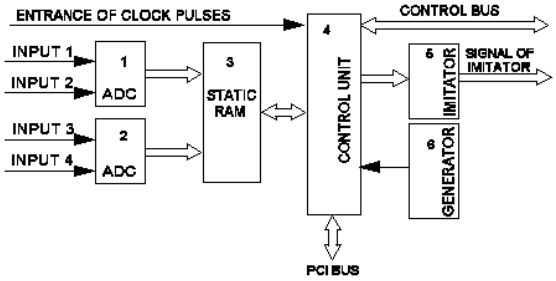

Fig. 1. Block diagram of the converter ADC-01

Scheme device consists of two 2-channel chip analog to digital converters ADC, operative static RAM memory, the control device, clock generator, simulator of signal.

Operation of the device is a synchronous converting analog electrical signals to the inputs of the 4 channels into digital form and recorded in a buffer memory. Sampling frequency of 10 or 20 MHz, 8 bit. Data are transferred to a PC via the PCI bus in MASTER mode after filling the memory of device. To digitize using two dual-chip ADCs AD9281 ANALOG DEVICES firm. Buffer memory is static with the recording time 12 ns (40 MHz). The logic of device implemented on the PLA ALTERA EPM3256ATC-144-10. Device sends eight bits of the address to the external switch that switches the sensor signals of a linear accelerator to input of device. Built- simulator of signals provides a test of the device.

Characteristics of device:

- a number of Bits 8;
- a frequency of discretisation 10, 20 MHz;
- static memory 512 byte in every channel;
- a delay of beginning of discretisation from 0.12.8 us.

Description of control bus:

- a number of bidirectional digits of bus of data - 8;
- two impulses of record in a register;
- an impulse of reading of data.

The device is a circuit board that is inserted into an available PCI slot of computer. A drivers this device and all subsequent devices of this family: ADC-02, ADC-03, ADC-05, ADC-06, allow to function in the operating systems of WINDOWS 98/2000/XP

Original appearance of device is shown on a Fig. 2.

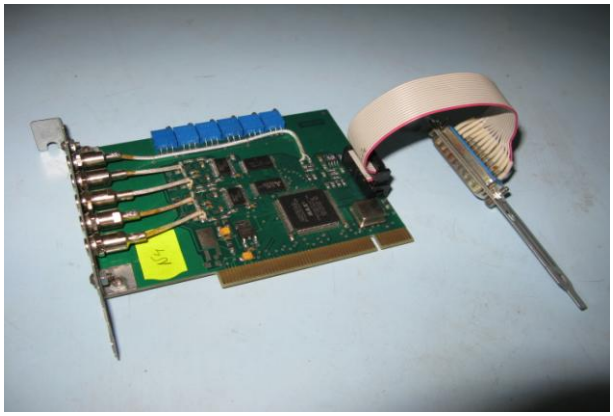

Fig. 2. Original appearance of device ADC-01

A device is applied in system of control and management of accelerators of LU- 10, LU-60M [1].

2. ANALOG-DIGITAL CONVERTER ADC-02

Setting, technical descriptions and principle of work are analogical to the device of ADC-01. To the device added a few extra features. The block diagram of the converter ADC-02 is shown in Fig. 3. The signaling processor and the executive relay are added to the scheme.

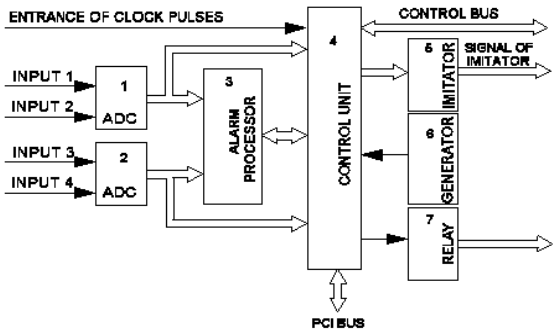

Fig. 3. Block diagram of the converter ADC-02

The signaling processor on a command from a computer calculates the difference of areas under of impulsive signals 1-th and 2-th, 3-th and 4-th channels, as

shown in Fig. 4. If entrance signals are value of currents of sensors on an entrance and exit of accelerating section of the linear accelerating that the difference of areas is proportional losses of charge of bunch of electrons in the accelerating section. If size of losses above the set value a device produces the signal of accident through a relay to the system control linear accelerator.

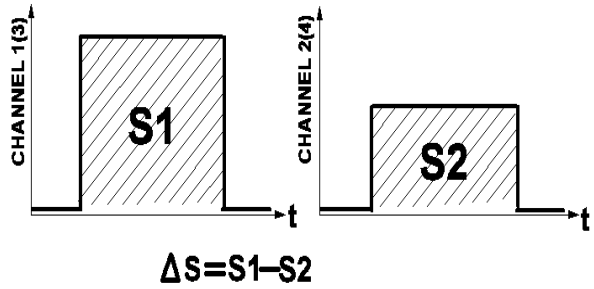

Fig. 4. Example of calculating the difference between the areas

Original appearance of device is shown on a Fig. 5.

Fig. 5. Original appearance of device ADC-02

A device is applied in system of control and management of accelerators of LU- 10, LU-60M [1].

3. ANALOG-DIGITAL CONVERTER ADC-03

The block diagram of the converter ADC-03 is shown in Fig. 6. Unlike devices ADC-01, ADC-02 is operated via a PC via CAN interface. CAN-bus controller mounted in the device for this.

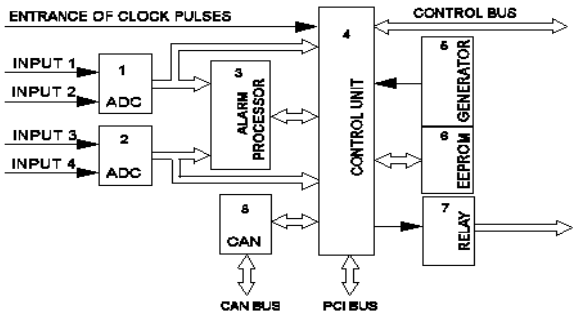

Fig. 6. Block diagram of the converter ADC-03

Principle of work and technical data are analogical to the device of ADC-01, ADC-02.

Original appearance of device ADC-03 is shown on a Fig. 7.

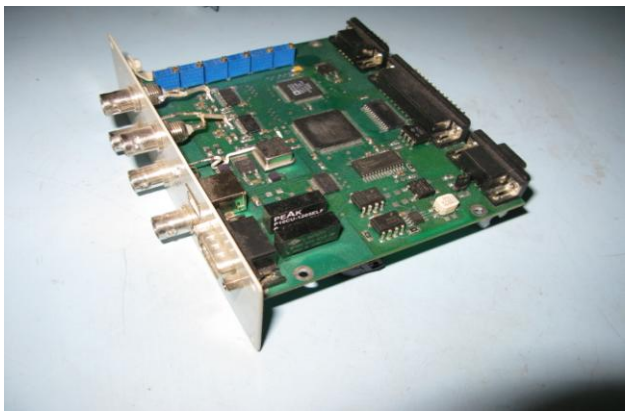

Fig. 7. Original appearance of device ADC-03

4. ANALOG-DIGITAL CONVERTER ADC-05

Block diagram of the converter ADC-05 is presented in Fig. 8.

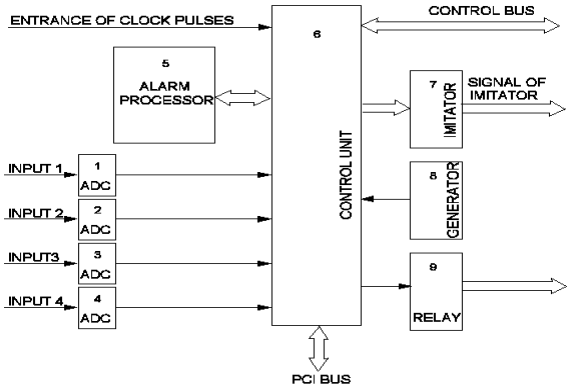

Fig. 8. Block diagram of the converter ADC-05

Four single chips ADC with a clock frequency of 100 MHz applied to the input of the device. Principle of work is analogical to the device of ADC-01, ADC-02, ADC-03. The device is operated via a PC via CAN-bus. Original appearance of device ADC-05 is shown on a Fig. 9.

Fig. 9. Original appearance of device ADC-05

5. ANALOG-DIGITAL CONVERTER ADC-06

Block diagram of the converter ADC-06 is presented in Fig. 10. The scheme of device is analogical to the device of ADC-05. To the scheme of device the microcircuit of EEPROM is added.

The device is controlled by a computer via CAN-bus. Technical data are similar to ADC-05.

Original appearance of device ADC-06 is shown on a Fig. 11.

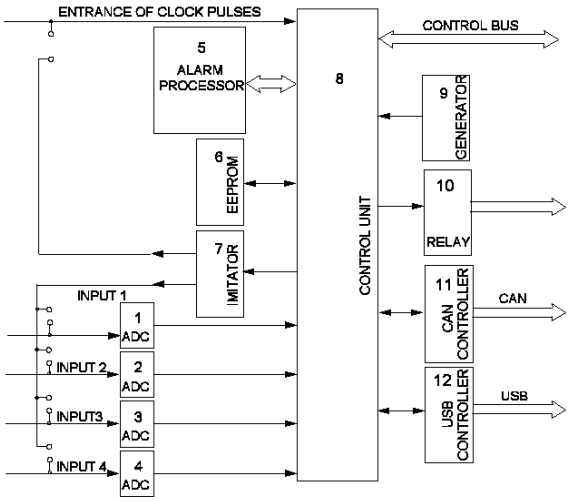

Fig. 10. Block diagram of the converter ADC-06

Fig. 11. Original appearance of device ADC-06

6. SYNCHRONIZER OF LINAC LU-60M

The synchronizer is used to control by parts of linear accelerators. An electric block diagram of synchronizer is conditionally broken on two parts 1 and 2 presented on Figs. 12 and 13.

Reductions applied are in a scheme:

-impulses BP1, BP2 are start-up pulses of klystrons 1 and 2;

-impulses VG are impulses start-up of leading generator;

-impulses MIE are impulses start-up the electron source;

-impulses SO are impulses start-up of control equipment on the stand of operator;

-impulses SC are impulses start-up of control equipment on the shield section;

-impulses BP3, BP4 are impulses reserve.

An amplitude out pulses of synchronizer 12 V, load current of 0.5 A.

Logical part of device is created on two programmable logical matrices (PLM) of type of ALTERA EPM3256ATC - 144-10 (on a block diagram the distinguished parts are under the names of ALTERA1 and ALTERA2). Both PLM function as single unit.

How does a device work? "CLOCK PULSE GENERATOR" generates a pulse frequency of 100 Hz. These pulses coincide in time with the zero crossing of the mains voltage These pulses are applied to the "REGULATOR OF PHASE" where their leading edges attached to the pulses of 10 MHz crystal oscillator. "SHAPER OF OPERATING FREQUENCIES" generates pulses with a frequency of 50, 25, 12.5, 6.25, 3.125, 1.041 Hz. Hereinafter referred to frequencies below 25 Hz, for simplicity will be designated as integers 1...12 Hz. Thus there is a grid of working frequency control linear accelerator 1...100 Hz, synchronized with the phase of the mains.

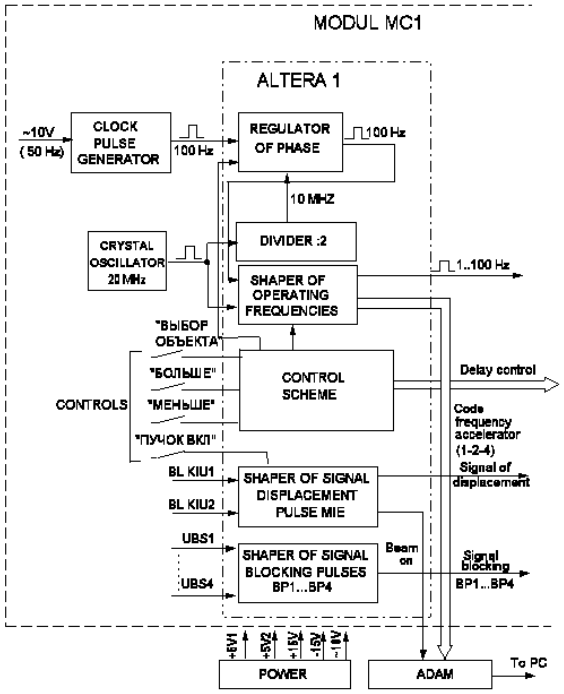

Fig. 12. Block diagram of synchronizer of LU-60M (part 1)

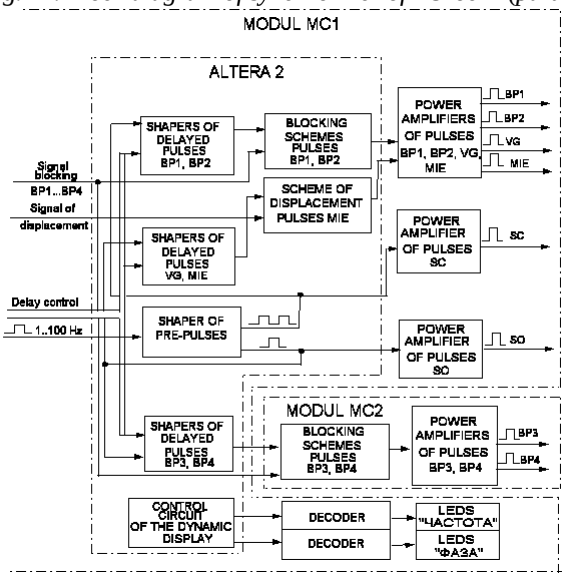

Fig. 13. Block diagram of the synchronizer of LU-60M (part 2)

Selecting the operating frequency is by the button "ВЫБОР ОБЪЕКТА" on the front panel of the synchronizer through "CONTROL SCHEME". Adjusting the reference clock phase 1...100 Hz controller implemented in the range from 0 to 9.9 ms to the supporting network with discrete steps of 10 ms using the buttons "БОЛЬШЕ", "МЕНЬШЕ" on the front panel of the synchronizer through the "CONTROL SCHEME" In the "SHAPER OF OPERATING FREQUENCIES" generated three-digit binary code of the selected frequency to control the frequency of the accelerator. This code and one digit-flag "included beam of accelerator" come through the serial port module "ADAM4051" to the

computer. If the accelerator operates at a frequency of 25 Hz and below to start forming line serves two pulses – pre-pulse plus working pulses. The time interval between pulses is 20 ms. Thes pulses are generated in the "SHAPER OF PRE-PULSE." Further, these pulses (in the block diagram shown as two pulses) are delivered in the "SHAPER OF DELAYED PULSES BP1, BP2". The single working pulses (without pre-) are delivered in the "SHAPER OF DELAYED PULSES VG, MIE", "SHAPER OF DELAYED PULSES SO", "SHAPER OF DELAYED PULSES BP3, BP4". Each channel provides a controlled delay at the output in the range 0...9.9 us in discrete steps of 0.1 us using the buttons "БОЛЬШЕ", "МЕНЬШЕ" on the front panel of the synchronizer.

Detainees pulses BP1...BP4, HS, MIE synchronization pulses SO for oscilloscopes and the impulses SS for panel of operator amplified by power amplifiers-shapers of the respective channels.

The block output pulses BP1...BP4 are in a synchronizer. Signals from UBS1...UBS4 (this subsystem of blocking of electron accelerator generates locking signals) enter in "SHAPER OF SIGNAL BLOCKING PULSES BP1...BP4". This scheme provides galvanic isolation of input signals. From the output of this circuit signals through "BLOCKING SCHEME PULSE BP1" and "BLOCKING SCHEME PULSE BP2" and similar schemes channels BP3 and BP4 blocking the flow of the delayed pulses at the amplifier-shapers channels BP1...BP4. If an emergency situation occurs in the work of the accelerator, then blocking the electron beam. "SHAPER OF SIGNAL DISPLACEMENT PULSE MIE" provides galvanic isolation of input signals from a subsystem of blocking of electron accelerator BLKIU1, BLKIU2. A signal displacement enters in "SCHEME DISPLACEMENT PULSE MIE". This scheme provides a displacement of pulse MIE to the 12 us relative to the working timing position. The electron beam is blocked until the intervention of staff.

"CONTROL CIRCUIT OF THE DYNAMIC DISPLAY" controls the operation of a digital LED displays.

Module MC-1 consists of a circuit board with the front panel, on which are the controls and LEDs.

Module MC-2 consists of a circuit board with the front panel, on which are LEDs.

The design of the synchronizer is a box, that includes modules MC-1, MC-2, power supply, controller "ADAM4051". Exterior view of the module MC1 is shown in Fig. 14.

Exterior view of a synchronizer accelerator LU-60M is shown in Fig. 15.

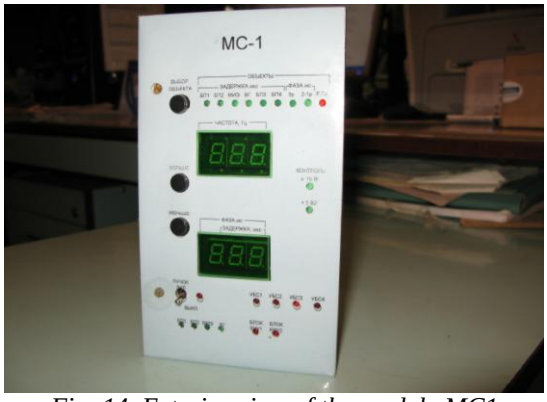

Fig. 14. Exterior view of the module MC1

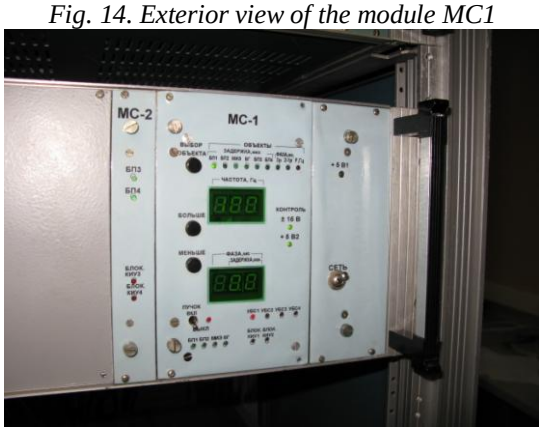

Fig. 15. Exterior view of the synchronizer accelerator LU-60M

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РАЗРАБОТКА НОВЫХ ЭЛЕМЕНТОВ АВТОМАТИЗИРОВАННЫХ СИСТЕМ УПРАВЛЕНИЯ ЛИНЕЙНЫМИ УСКОРИТЕЛЯМИ

В.Н. Борискин, В.А. Ляховец, А.А. Сарвилов, В.А. Момот, А.Н. Савченко, Г.Н. Цебенко, В.В. Верещака

Для систем контроля и управления линейными ускорителями электронов были разработаны, изготовлены и внедрены новые элементы взамен физически и морально устаревших. Это – семейство аналого-цифровых преобразователей типа ADC-01, ADC-02, ADC-03, ADC-05, ADC-06 было разработано совместно с сотрудниками ХНУРЭ, а также синхронизатор для линейного ускорителя ЛУЭ-60М, разработанный силами сотрудников научно-исследовательского комплекса (НИК) "УСКОРИТЕЛЬ" ННЦ ХФТИ. Представлены технические описания, краткие характеристики, структурные схемы и внешний вид преобразователей и синхронизатора.

РОЗРОБКА НОВИХ ЕЛЕМЕНТІВ АВТОМАТИЗОВАНИХ СИСТЕМ УПРАВЛІННЯ ЛІНІЙНИМИ ПРИСКОРЮВАЧАМИ

В.М. Борискін, В.О. Ляховець, О.А. Сарвілов, В.О. Момот, А.М. Савченко, Г.М. Цебенко, В.В. Верещака

Для систем контролю і управління лінійними прискорювачами електронів було розроблено, виготовлено та впроваджено нові елементи замість фізично і морально застарілих. Це – сімейство аналого-цифрових перетворювачів типу ADC-01, ADC-02, ADC-03, ADC-05, ADC-06, розроблених спільно із співробітниками ХНУРЕ, а також синхронізатор для лінійного прискорювача ЛУЕ-60М, розроблений силами співробітників науково-дослідного комплексу (НДК) "ПРИСКОРЮВАЧ" ННЦ ХФТІ. Представлено технічні описи, короткі характеристики, структурні схеми та зовнішній вигляд перетворювачів та синхронізатора.