Effect of dislocations in relaxed MBE SiGe layers on the electrical behavior of Si/SiGe heterostructures

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Defects in Si/SiGe heterostructures and electrical behavior thereof have been studied. Misfit dislocations were observed in the epitaxial layers using cross-sectional transmissi on electron microscopy. These defects cause anomalies in the electrical behavior. It has been shown that, in spite of anomalies, the electrical measurements provide useful and reliable information on the structures.

Исследованы дефекты в гетероструктурах Si/SiGe и их электрические характеристики. В эпитаксиальных слоях методом просвечивающей электронной микроскопии поперечных сечений обнаружены дислокации несоответствия. Эти дефекты вызывают аномалии в электрических характеристиках. Показано, что, несмотря на эти аномалии, электрические измерения обеспечивают полезную и надежную информацию о структурах.

In this work, the electrical behaviour of Al/n-SiGe/n-Si heterojunctions prepared using two different surface treatments have been studied as a function of temperature. Due to the different surface treatments, one type of the structures exhibit a low Schottky barrier height while the other type, a relatively high one. Although anomalous temperature dependences of the electrical behaviour have been obtained, the prepared Schottky junctions with significantly different barrier heights have proved a very useful tool for studying the effect of dislocations formed during the epitaxial growth. In spite of anomalies, useful information and reliable parameters have been obtained from the electrical measurements.

The SiGe layers were grown by MBE with solid phase Si and gas phase GeH_4 sources on n^+Si substrates [1, 2]. The substrate temperature was 700°C, the sublimation temperature of Si 1320°C, the GeH_4 pressure in the reactor chamber 0.5 mTorr [1]. The growth rate was 10–15 nm/min. First, a 0.8 μm thick Si buffer layer was grown. Two wafers were studied with Ge content in the SiGe layer of 0.11 and 0.20, respectively. The SiGe layer thickness was about 200 and 240 nm, respectively, with a free electron concentration of $3\cdot10^{15}$ cm^{-3}. The wafers were cut into two parts and Al Schottky junctions were formed on the the wafer front sides using two different surface treatments prior to Al evaporation. These treatments were applied to Si in our earlier work [3]. The "HF" treatment which is standard in our Si technology consisted of two steps: 1) Cleaning in 1:1 solution of H_2SO_4 and H_2O_2 for 30 min. 2) Etching in 1:40 solution of HF and H_2O for 1 min. The

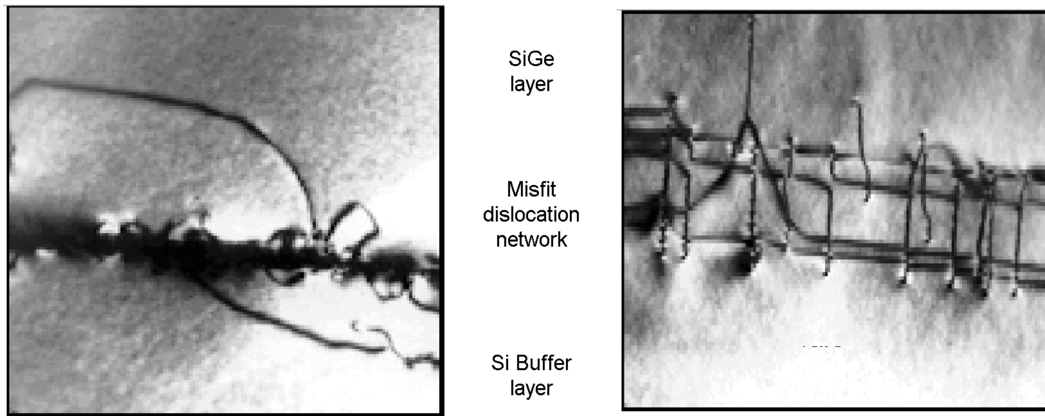

Fig. 1. The misfit dislocation network obtained by XTEM measurements for two different areas of the studied heterostructures: left, 5.0 μm by 4.5 μm; right, 1.7 μm by 1.5 μm.

"$H_2SO_4 + H_2O_2$" treatment consisted of steps 1) and 2) of the standard HF treatment, and as a third step, step 1) was repeated for 15 min. After the actual surface treatment, Al was evaporated onto the front side for Schottky junctions to be studied. For the backside ohmic contacts, also Al was used after $H_2SO_4 + H_2O_2$ treatment. This treatment yields a very good ohmic contact to n-Si [3]. Square diodes of 0.64 mm^2 size were formed on the front side of the wafers by standard photolithography.

The defect structure in SiGe/Si heterostructures was investigated by cross-sectional transmission electron microscopy (XTEM). The electrical characteristics were studied by d.c. current-voltage (I-V) measurements, and capacitance voltage (C-V) and conductance-voltage (G-V) measurements at a frequency of 1 MHz in the temperature range of 80–320 K in darkness. The I-V characteristics were interpreted according to thermionic emission theory.

An extended misfit dislocation network has been detected at the SiGe/Si interfaces by XTEM measurements as shown in Fig. 1.

For the HF treatment, a Schottky barrier height of 0.73±0.03 eV has been obtained which is close to 0.76 eV value obtained for n-Si [3]. The barrier height obtained for the $H_2SO_4 + H_2O_2$ treatment was 0.46±0.04 eV, which is much higher than that for n-Si (less than 0.15 eV [3]).

The electrical behaviour exhibit various anomalies. The forward I-V characteristics show excess currents, but below room temperature only, as shown in Fig. 2 which presents typical forward I-V characteristics of junctions on wafer with Ge content of 0.20 prepared using both surface treatments. For

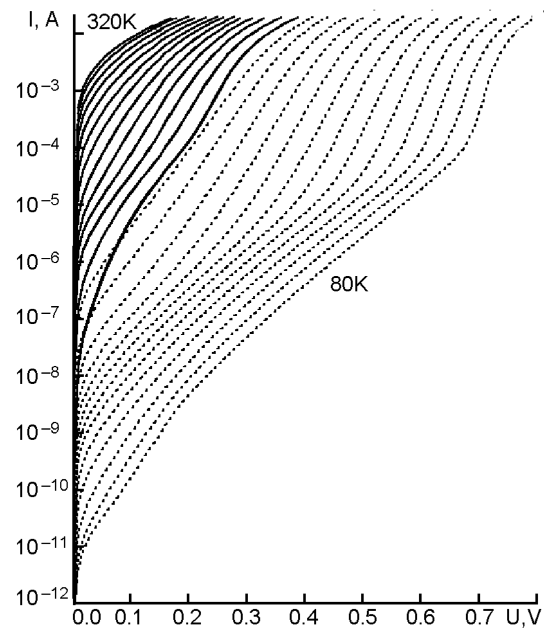

Fig. 2. Typical forward I-V characteristics as a function of temperature for junctions on wafer with Ge content of 0.20 prepared with HF (dotted lines) and $H_2SO_4 + H_2O_2$ (solid lines) treatment.

the wafer with Ge content of 0.11, similar characteristics were obtained [2]. The forward excess currents for both wafers depend strongly on temperature, so those were attributed to the thermionic-field emission connected with the electric field enhancement near dislocations [4]. Crystal defects usually yield excess or leakage currents [5], as it was also obtained recently for InP [6, 7] and AlAs/GaAs [8] Schottky and InAs/GaAs quantum well structures [8].

The wafers with Ge content of 0.11 and 0.20 exhibit similar behaviour, the only significant difference is observed in the tem-

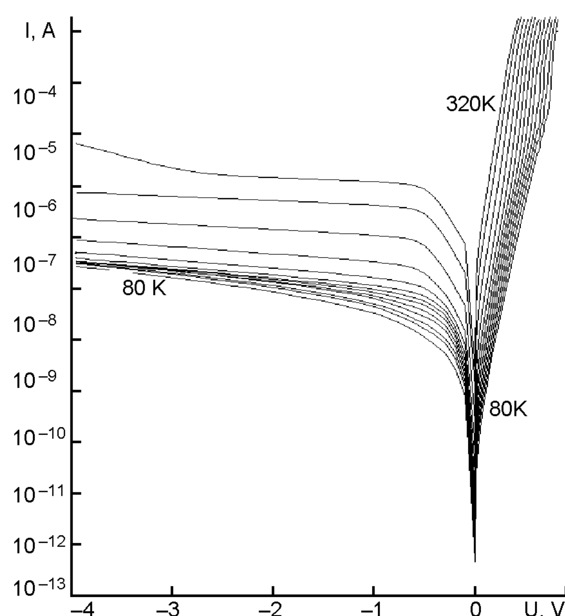

Fig. 3. Typical forward and reverse I-V characteristics as a function of temperature for junctions on wafer with Ge content of 0.11 prepared with HF.

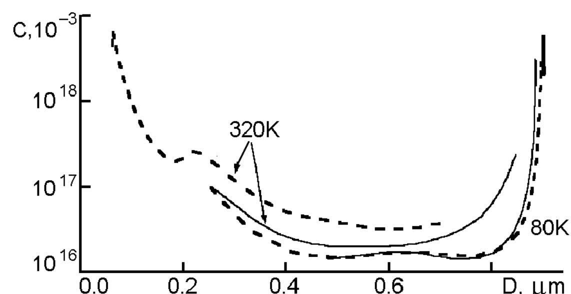

Fig. 4. The apparent doping profiles for junctions on wafer with Ge content of 0.11 with Schottky barrier heights of 0.46 eV (solid lines) and 0.73 eV (dashed lines) (HF and $H_2SO_4 + H_2O_2$ treatments, respectively), obtained at 80 and 320 K.

perature dependences of their I-V characterisitics as shown in Fig. 3. The reverse current through junctions on wafer with Ge content of 0.11 depends on temperature very weakly below 220 K. This indicates that the actual current mechanism at these temperatures is the field emission as it was also found recently for *n*-type InP Schottky junctions [6, 12].

A strong increase of reverse current is obtained in junctions with HF treatment on both wafers for low reverse biases, as shown in Fig. 3. This strong bias dependence indicates a recharging process within the junction which affects the barrier height.

The ideality factor and apparent barrier height obtained from the steep part of the I-V characteristics depends on the temperature for both wafers and both surface treatments [2]. This effect can be connected either with the lateral inhomogeneity of barrier height or with the predomination of the current with thermionic field emission [9, 10]. In the studied structures, both mechanisms may be valid. Dislocations yield probably an inhomogenous electric field and potential barrier height at the interface, on one hand, and enhanced electric fields can result in anomalously high level of thermionic-field emission. However, the temperature dependence of ideality factor and apparent I-V barrier height can be simply connected with the common effect of the excess current and series resistance on the slope of the linear regions of semilogarithmic I-V characteristics. As the excess current is strongly temperature dependent, its effect on the linear region slope depends on temperature as well [11] (see Fig. 2).

The C-V barrier heights also increase with increasing temperature [2] for both wafers and both surface treatments which is unusual for *n*-type Schottky junctions [13]. This feature can be due to the temperature dependence of interface charge. There is also a significant difference between the apparent I-V and C-V barrier heights [2]. The latter is lower, which suggests a large positive charge near the interface, e.g. a thin heavily doped ionized *n*-type layer at the SiGe surface [10, 14, 15]. The indications of such a layer were also obtained by evaluation of doping profiles from the C-V measurements presented in Fig. 4.

C-V characteristics exhibit very strong temperature dependence for the studied junctions with $H_2SO_4 + H_2O_2$ treatment (low barrier height), as shown in Fig. 5. There is also an abrupt change of the capacitance near zero bias, which also indicates a recharging process close to the Al/SiGe interface. Further on, the C-V characteristics exhibit a switching behaviour with a hysteresis at moderate forward biases as well, as also shown in Fig. 5. Junctions with low barrier height exhibit high conductance at room temperature as well [2]. The junctions with HF treatment (high barrier height) do not exhibit high conductance at any temperature.

The free electron profiles evaluated from the C-V characteristics of both type of junctions (HF and $H_2SO_4 + H_2O_2$ treatments) are presented in Fig. 4 for 80 and 320 K.

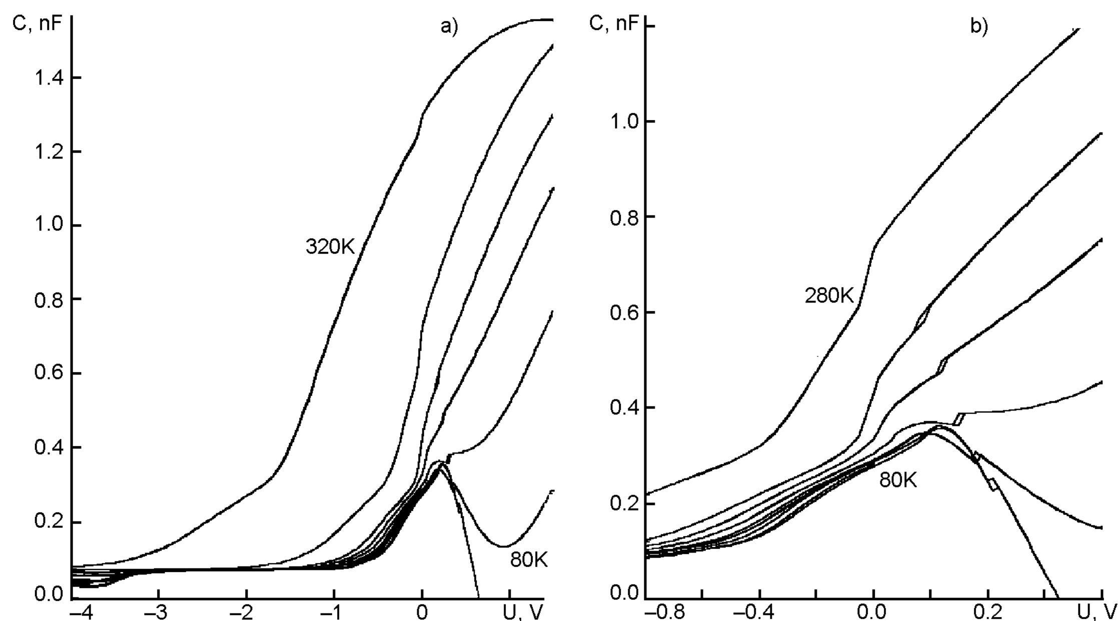

Fig. 5. Typical capacitance-voltage characteristics of junctions on wafer with a Ge content of 0.11 prepared with $H_2SO_4 + H_2O_2$ treatment, as a function of temperature. Note the different capacitance and bias scales for (a) and (b).

The profiles obtained for junctions with higher barrier height for both temperatures are reliable, as the conductance of these junctions is low. The same is true for the profile obtained for the junction with low barrier height at 80 K. The similarity of the profiles suggests that the profile obtained for junction with low barrier height at 320 K is also reliable, and contains useful information. The peak at a depth of 0.2 μm corresponds to the misfit dislocations at the SiGe/Si interface.

A more detailed analysis of the electrical characteristics of SiGe/Si structures will be presented elsewhere [2].

Thus, the defects in SiGe/Si heterostructures and their electrical behaviour have been studied. The defects have been found to affect strongly the electrical properties. Those yield excess currents due to the electric field increase around the defects resulting in thermionic-field emission or field emission currents. Those may yield instabilities in the C-V behaviour. The defects affect also the C-V and G-V behaviour yielding in some cases their anomalous temperature dependence and an anomalous apparent barrier height (anomalous voltage intercept of the Schottky-Mott plot). It has also been obtained that in spite of anomalies of the electrical behaviour, electric measurements provide useful and reliable information about the structures.

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Вплив дислокацій у релаксованих шарах SiGe на електричні характеристики гетероструктур Si/SiGe

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Досліджено дефекти у гетероструктурах Si/SiGe та їх електричні характеристики. В епітаксиальних шарах методом просвічувальної електронної мікроскопії поперечних перерізів виявлено дислокації невідповідності. Ці дефекти спричиняють аномалії в електричних характеристиках. Показано, що, незважаючи на ці аномалії, електричні вимірювання забезпечують корисну та надійну інформацію про структури.