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Accurate numerical modelling the GaAs MESFET current-voltage characteristics

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Abstract. In this paper, we present a computing model of the current-voltage (*I-V*) characteristics of a gallium arsenide Schottky barrier field effect transistor called GaAs MESFET. This physical model is based on the two-dimensional analysis of the Poisson equation in the active region under the gate. In this frame, we elaborated a simulation software based on analysis of expressions that we have previously set up [1-3], the obtained theoretical results are discussed and compared to the experimental ones.
Keywords: gallium arsenide, field effect transistor, Poisson equation.

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1. Introduction

Essentially, the Gallium Arsenide Field Effect Transistors (GaAs FET) are high-speed and high-frequency devices. In this paper, we propose a simulation of the current-voltage (*I-V*) characteristics of a short-gate GaAs MESFETs. Computer-aided analysis is a useful technology for studying physical phenomena in semiconductors. Here, we presented two-dimensional simulation of GaAs MESFET considering the physical model. Two-dimensional solution of the Poisson equation has been obtained taking into account structure study results.

2. Physical model

Fig. 1 shows a normal planar GaAs MESFET simulated in this paper. Two-dimensional physical model is used to solve the Poisson equation. This equation known in semiconductor physics is used in all the models to explain the different physical phenomena specific to the GaAs MESFET [4-6].

But the main problem for these models lies in the coupling of partial and nonlinear differential equations, which require to be simultaneously solved. The difficulty of putting down a valid hypothesis for the limit conditions at the free interface requires the resort to approximations the negligence of a certain number of terms that act negatively on the model exactness [4-6].

In this paper, we present an analytical model that combines the description of physical phenomena and simplicity of solving the respective mathematical equation.

3. Determination of the two-dimensional voltage in the active region

The two-dimensional solution of differential equations using the Green method gives a distribution of the electric field under the region of the space charge area (SCA). The general Poisson equation is given by

$$\Delta V_c(x,y) = \frac{\partial^2 V_c}{\partial x^2} + \frac{\partial^2 V_c}{\partial y^2} = \frac{-\rho(x,y)}{\varepsilon}. \qquad (1)$$

To calculate the voltage under the gate, the SCA is divided into two main regions shown in Fig. 1.

- The region (1) is directly under the gate, it is considered as a region controlled by the gate. We use the uni-dimensional approximation to calculate the composant of the relation of the voltage $V_q(x,y)$ specific to this region.
- The region (2) outside the first region is considered as uncontrolled by the gate. The two-dimensional voltage of the channel under the gate is given as follows:

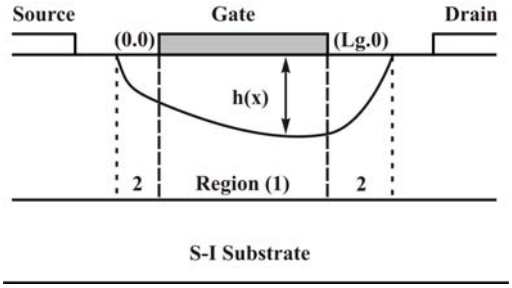

Fig. 1. Depletion regions controlled (1) and uncontrolled (2) by the gate.

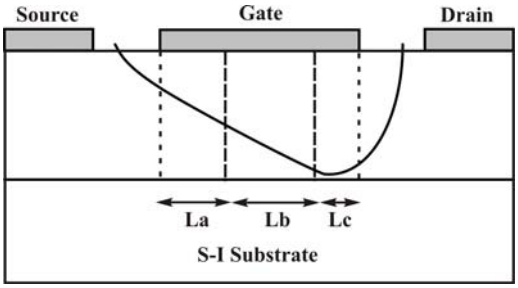

Fig. 2. Active area distribution according to the electric field variation.

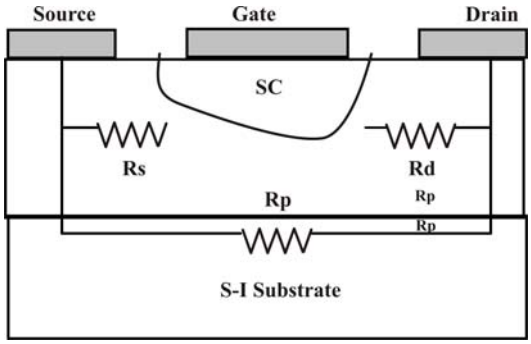

Fig. 3. Parasitic resistance of GaAs MESFET.

$$V_c(x,y) = V_q(x,y) + V_l(x,y)\,, \tag{2}$$

where

$$V_q(x,y) = \int_0^y \frac{eN_d(x,y)}{\varepsilon} y dy + y\int_y^{h(x)} \frac{eN_d(x,y)}{\varepsilon} dy + V_{bi} + V_g\,, \tag{3}$$

and

$$V_l(x,y) = \left[A_1^s \frac{\sinh\left(k_1(L-x)\right)}{\sinh\left(k_1 L\right)} + A_1^d \frac{\sinh\left(k_1 x\right)}{\sinh\left(k_1 L\right)} \right] \sin\left(k_1 y\right) \tag{4}$$

with

$$A_1^s = \frac{2}{a}\int_0^a \left[V_c(0,y) - V_q(0,y)\right] \sin(k_1 y) dy \tag{5}$$

and

$$A_1^d = \frac{2}{a}\int_0^a \left[V_c(L,y) - V_q(L,y)\right] \sin(k_1 y) dy\,. \tag{6}$$

A_1^d and A_1^s are the Fourier coefficients for the gate supplementary voltage for the drain and source sides, respectively [5],

and $k_1 = \dfrac{\pi}{2a}$.

If considering (3) and (4), the total voltage expression becomes

$$V_c(x,y) = \int_0^{h(x)} \frac{eN_d(x,y)}{\varepsilon} y dy + V_l(x,y) - V_g + V_{bi}\,. \tag{7}$$

4. Current-voltage characteristics

To calculate the drain current expression as a function of the drain voltage for different values of the gate voltage, we use the following hypothesis:

- we neglect the current in the *Y*-axis, this approximation is valid for the short-gate components;
- we suppose the electrons mobility constant;
- we derived the channel in three regions according to the electric field value (Fig. 2) [6].

5. Determination of the current general equation

To calculate the drain current general equation, we used the uni-dimensional approximation to simplify the mathematical expressions. We also use the following expressions:

$$\vec{J}_x = -e\mu_n N_d(y) E_x = -e\mu_n N_d \frac{dV}{dx}\,, \tag{8}$$

the drain current expression is given by

$$I_d = -\int_{(s)} J_x ds = -Z\int_{h(x)}^{a} J_x dy\,, \tag{9}$$

using single integrals, the current expression is obtained by relation

$$I_d = \frac{(eN_d)^2 Z\mu_n}{\varepsilon L}\left[\frac{a}{2}(h_d^2 - h_s^2) - \frac{1}{3}\left(h_d^3 - h_s^3\right)\right] \tag{10}$$

where

$$h_s = \left[\frac{2\varepsilon}{eN_d}\left(V_{bi} - V_g\right)\right]^{1/2}\,, \tag{11a}$$

$$h_d = \left[\frac{2\varepsilon}{eN_d}\left(V_d + V_{bi} - V_g\right)\right]^{1/2} \tag{11b}$$

are the widths of the space charge area (SCA) respectively source side and drain side.

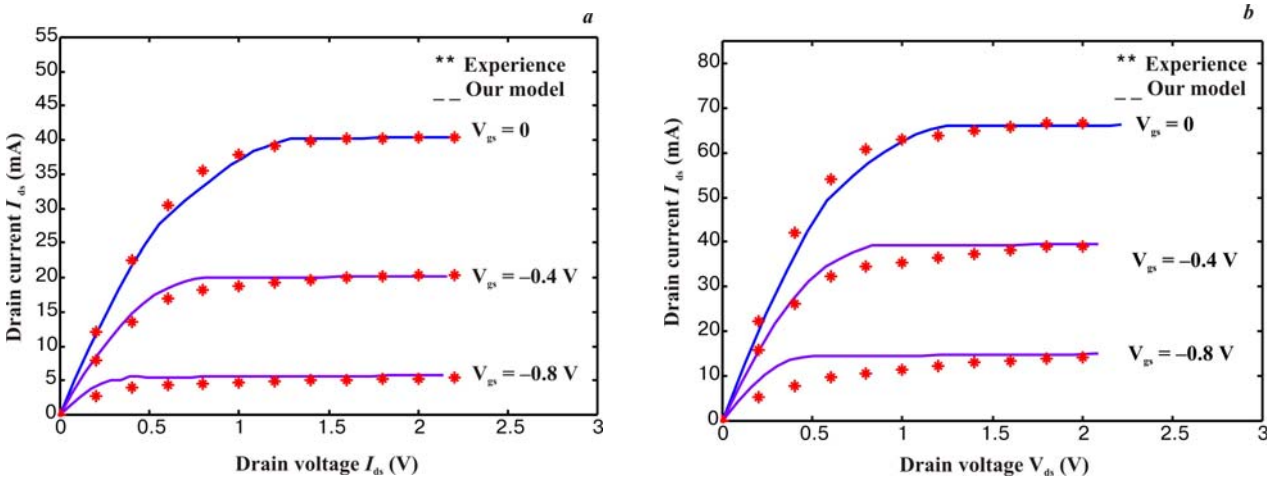

Fig. 4. Comparison of the *I-V* characteristics measured and calculated by the simulation for MESFETs 1 (a) and 2 (b).

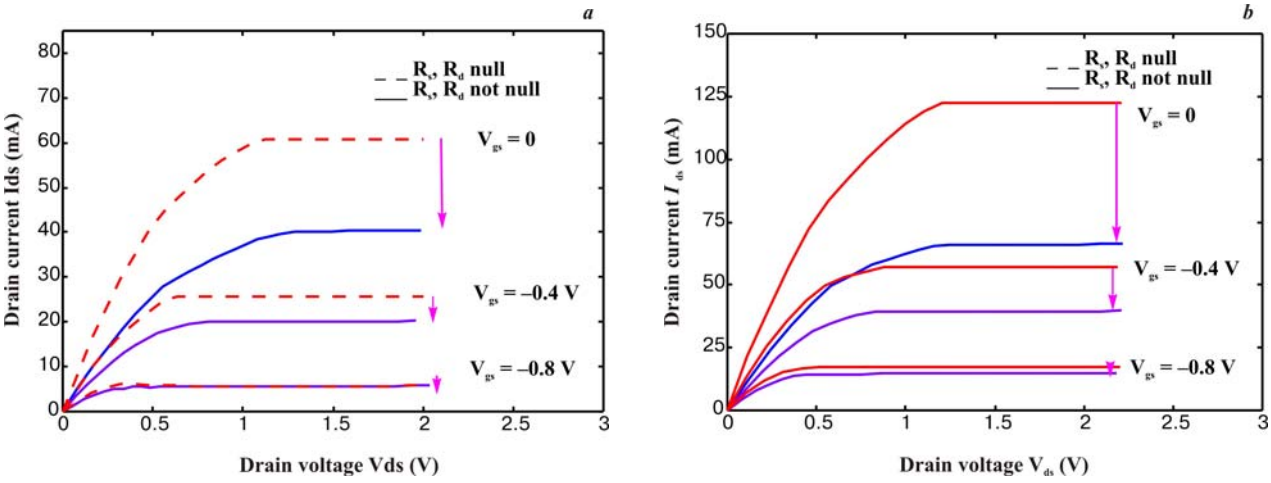

Fig. 5. Effect of the parasitic resistances on the *I-V* characteristics for MESFETs 1 (a) and 2 (b).

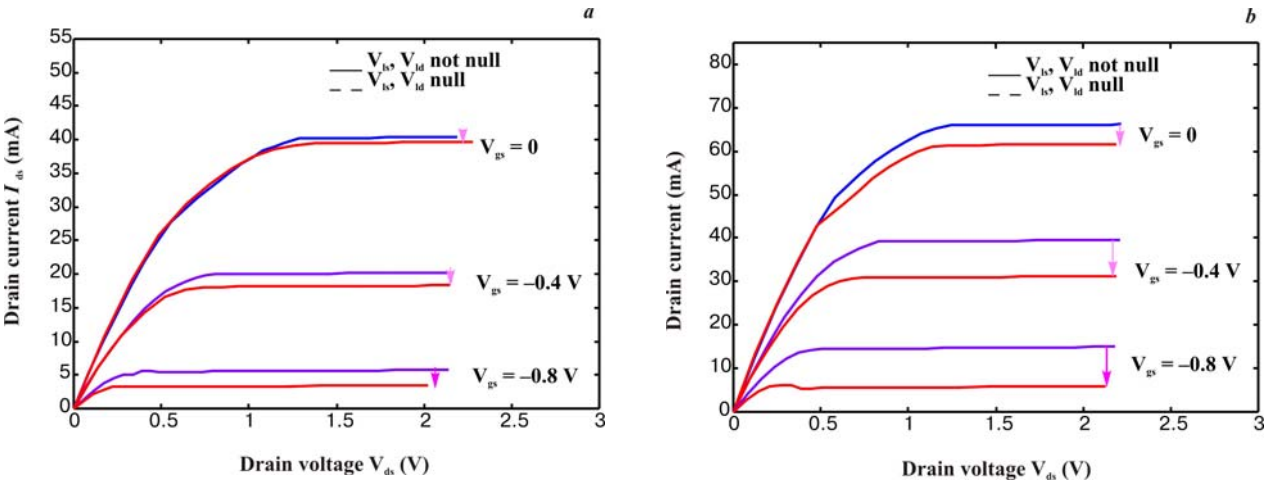

Fig. 6. Effect of the side voltages V_{ls} and V_{ld} on the *I-V* characteristics for MESFETs 1 (a) and 2 (b).

Defining the pinch-off current I_p is given by

$$I_p = \frac{(eN_d)^3 Z\mu a^3}{2\varepsilon L} \quad (12)$$

and the pinch-off voltage V_p is given by

$$V_p = \frac{eN_d}{2\varepsilon}a^2 . \quad (13)$$

The general equation expression I_P in the channel becomes

$$I_d = I_p\left[\frac{V_d}{V_p} - \frac{2}{3}\left(\frac{V_d + V_{bi} - V_g}{V_p}\right)^{3/2} + \frac{2}{3}\left(\frac{V_{bi} - V_g}{V_p}\right)^{3/2}\right]. \quad (14)$$

6. Effect of the mobility law

The hypothesis of the constant mobility and the independency of the electric field in the *n*-type GaAs can not convey the physical phenomena. The analytical expression of the mobility variations with the electric field used by us is a simplified relation [7, 8] given as follows:

- for the weak electric field where $E < E_0$
  $\mu = \mu_0$; (15a)
- for the high electric field beyond E_0 ($E > E_0$)

$$\mu = \frac{\mu_0}{\left[1 + \left(\frac{E - E_0}{E_s}\right)^2\right]^{1/2}} . \quad (15b)$$

This mobility law allows to obtain the different expressions of the drain current in different operation regimes.

I_d (V_d,V_g) characteristics of the GaAs MESFET corresponding to different operation regimes obey the equations considered below.

Table 1.

Transistor	L, μm	A, μm	Z, μm
MESFET 1	1	0.153	300
MESFET 2	0.5	0.1435	300
Transistor	μ_0, $m^2/V\cdot s$		N_d, $10^{23}m^{-3}$
MESFET 1	0.4000		1.17
MESFET 2	0.4000		1.31
Transistor	V_s, m/s	V_{bi},V	V_p,V
MESFET 1	$3.6\cdot10^3$	0.85	1.93
MESFET 2	$7.3\cdot10^3$	0.85	1.93

Table 2.

Transistor	a_1	b_1	c_1	V_l/V_p
MESFET 1	–0.10	0.10	0.05	0.01
MESFET 2	–0.14	0.10	0.04	0.01

6.1. Linear regime

This regime exists as far as L_a occupies all the channel, it corresponds to the weak field area where the mobility is equal to μ_0.

The drain current expression in this regime is given as

$$I_d = I_{pl}\left[\frac{V_d}{V_p} - \frac{2}{3}\left(\frac{2}{3}\frac{V_d + V_{bi} - V_g}{V_p}\right)^{3/2} + \frac{2}{3}\left(\frac{V_{bi} - V_g}{V_p}\right)^{3/2}\right] \quad (16)$$

where

$$I_{pl} = \frac{e^2 {N_d}^2 Z\mu_0 a^3}{2\varepsilon L_a} .$$

6.2. Pinch-off regime

As the drain voltage increases, the electric field in the channel increases beyond E_0 .The channel under the gate can be then represented by two regions.

One region of the length L_a in which the field is inferior to E_0 and the electron mobility is constant and given by $\mu = \mu_0$. Another region of the length L_b ($L = L_a + L_b$) in which the field is superior to the field E_0 but inferior to the field E_m, and the electron mobility is given by the expression (15b).

First region**:** for $E < E_0$ and $0 < x < L_a$

$$L_a = \frac{I_{pl}L}{I_d}\left[\frac{V_{da}}{V_p} - \frac{2}{3}\left(\frac{V_{da} + V_{bi} - V_g}{V_p}\right)^{3/2} - \frac{2}{3}\left(\frac{V_{bi} - V_g}{V_p}\right)^{3/2}\right]. \quad (17)$$

Second region**:** for $E_0 < E < E_m$ and $L_a < x < L$

$$L_b = \frac{I_{ps}L}{I_d}\left[\frac{V_d - V_{da}}{V_p} - \frac{2}{3}\left(\frac{V_d + V_{bi} - V_g}{V_p}\right)^{3/2} + \left(\frac{V_{da} + V_{bi} - V_g}{V_p}\right)^{3/2}\right] \quad (18)$$

where

$$I_{ps} = \frac{I_p}{\left[1 + \left(\frac{E - E_0}{E_s}\right)^2\right]^{1/2}} .$$

6.3. Saturation regime

In this case, the channel under the gate is divided into three regions L_a, L_b, and L_c where $L = L_a + L_b + L_c$.

$$L_a = \frac{I_{pl}L}{I_d}\left[\frac{V_{da}}{V_p} - \frac{2}{3}\left(\frac{V_{da} + V_{bi} - V_g}{V_p}\right)^{3/2} - \frac{2}{3}\left(\frac{V_{bi} - V_g}{V_p}\right)^{3/2}\right], \quad (19)$$

$$I_b = \frac{I_{ps}L}{I_d}\left[\frac{V_{dm}-V_{da}}{V_p} - \frac{2}{3}\left(\frac{V_{dm}+V_{bi}-V_g}{V_p}\right)^{3/2} + \frac{2}{3}\left(\frac{V_{da}+V_{bi}-V_g}{V_p}\right)^{3/2}\right], \quad (20)$$

$$I_c = \frac{I_{ps}L}{I_d}\left[\frac{V_d-V_{dm}}{V_p} - \frac{2}{3}\left(\frac{V_d+V_{bi}-V_g}{V_p}\right)^{3/2} + \frac{2}{3}\left(\frac{V_{dm}+V_{bi}-V_g}{V_p}\right)^{3/2}\right] \quad (21)$$

where V_{da} and V_{dm} are successively maximum and pinch-off voltages for linear regimes.

7. Effect of the voltage $V_l(x, y)$

The effect of the voltage $V_l(x,y)$ is taken into consideration in the following expressions of the drain and gate voltages:

$$V_d \to V_d + V_{ld} \text{ and } V_g \to V_g + V_{ls} \quad (22)$$

where

$$V_{ls} = V_l(0, h_s) = A_1^s \sin\left(\frac{h_s\pi}{2a}\right), \quad (23a)$$

$$V_{ld} = V_l(L, h_d) = A_1^d \sin\left(\frac{h_d\pi}{2a}\right). \quad (23b)$$

The coefficient expressions A_1^s and A_1^d are very complex [6], they are essentially related to the polarization voltages V_d and V_g and to the voltages V_{bi} and V_p:

$$A_1^s = V_p\left[a_1 + b_1\left(\frac{V_{bi}-V_g-V_l}{V_p} - c_1\right)^{1/2}\right], \quad (24a)$$

$$A_1^d = V_p\left[a_1 + b_1\left(\frac{V_d+V_{bi}-V_g-V_l}{V_p} - c_1\right)^{1/2}\right]. \quad (24b)$$

For uniform doping, the coefficients a_1, b_1, c_1, and V_l are constants.

8. Effect of parasitic elements

The characteristics that we have presented are those concerning internal or intrinsic dimensions (I_d, V_d, V_g). To obtain the external or extrinsic characteristics (I_{ds}, V_{ds}, V_{gs}) of the component, we have to take into consideration the effect of the parasitic access source resistance R_s, the drain resistance R_d and also the effect of the resistance R_p parallel to the channel on the polarization voltages values (Fig. 3).

To obtain the real expressions of the characteristics $I_{ds}(V_{ds}, V_{gs})$, we have to substitute the intrinsic terms by the extrinsic terms in all the previous relations. Therefore

$$V_d = V_{ds} + V_{ld} - (R_s + R_d)I_d, \quad (25a)$$

$$V_g = V_{gs} + V_{ls} - R_s I_d, \quad (25b)$$

$$I_d = I_{ds} - (V_d/R_p). \quad (25c)$$

9. Results and discussion

In order to validate the *I-V* characteristics of the GaAs MESFET set up in the previous work, a simulation software based on different formulas and equations is exposed, as well as the obtained results and their discussions.

The numerical calculation of the drain current as a function of the polarization voltage calls the expressions (16) - (21) previously established.

The study has been carried out on two MESFET 1 and MESFET 2 [6] parameters of which are summarized in the following Table 1. To calculate the voltages V_{ld} and V_{ls} (expressions (23a) and (23b)), the values of the used parameters a_1, b_1, c_1, and V_l/V_p are tabulated in the Table 2.

In order to check the validity of our model, we have compared the theoretical results with the experimental ones for the MESFET 1 and MESFET 2.

In Figs 4a and b, we have respectively represented the comparison of the measured $I_{ds}(V_{ds},V_{gs})$ characteristics and the calculated ones by the simulation for the MESFET 1 and MESFET 2. In the linear regime, i.e., at a weak drain voltage polarization, we notice a good agreement between the experimental values and the simulation ones for both transistors. When the drain voltage increases and becomes more important, we notice a certain difference between the experimental values and the results of the simulation. This difference progressively increases until the saturation. This difference is mainly caused by the approximations made in the mathematical model and the simulation software, it also stems from the geometric parameters effects and existence of parasitic quantum phenomenon, which we have not taken into consideration. In the saturation regime, when the drain voltage gets important, we notice that the theoretical results are in a good agreement with experimental ones. In conclusion, we also remark that the theoretical and the experimental results have the similar behavior towards the drain voltage and coincide well, notably at high values of the V_{ds} voltage. This shows that the method is well founded.

- **Effect of source and drain parasitic resistances**

In order to put into evidence the effects of the source and drain parasitic resistances R_s and R_d on the *I-V* characteristics of the GaAs MESFET, in Figs 5a and b, in the case of the previous two transistors, we present the variations of the drain current as a function of the drain voltage with and without the parasitic resistance.

- **Effect of the voltage $V_l(x, y)$**

When solving the two-dimensional Poisson equation, it should be taken into consideration two voltages existing at the sides of the conducting channel: V_{ls} source side and V_{ld} drain side. Despite their very

weak values, these voltages influence the *I-V* static transistor characteristics. In Figs 6a and b, we present the effect of these side voltages for two studied structures.

10. Conclusion

In this paper, we have proposed an analytical study of the *I-V* characteristics of the GaAs MESFET. The influence of parasitic elements and sides voltages V_{ls} and V_{ld} on the drain current I_{ds} expression has been established, these latest voltages resulted from the two-dimensional analysis of the Poisson equation by the Green technique. This study allowed us to carry out a synthetic approach to this two-dimensional analysis to realize a valid exactness of the analytical model for static characteristics of the GaAs MESFET composant.

References

1. S. Khemissi, *Master thesis* // Faculty of Sciences, Constantine University (2003).
2. N. Merabtine, *Ph.D thesis* // Faculty of Engineering, Constantine University (2003).
3. M. Zaabat. *Ph.D thesis* // Faculty of Technology, Oum El Bouaghi University (2004).
4. J. Haslett *et al.* // *IEEE Trans. Electron. Devices* **47** (5) (2000).
5. H. Tran *et al.* // *Ibid.* **39** (9) (1992).
6. B. Janiguez *et al.* // *Ibid.* **46** (8) (1999).
7. S.P. Chin, C.Y. We // *Ibid.* **40** (4) (1993).
8. K.M. Shin, D.P. Klamer, J.I. Lion // *Solid State Electronics* **35** (11) (1992).
9. C.S. Chang, D.Y. Day // *IEEE Trans. Electron. Devices* **36** (2) (1989).
10. S.P. Murray, K.P. Roenker // *Solid State Electronics* **46** (2002).