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Novel hysteresis effect in ultrathin epitaxial Gd_2O_3 high-*k* dielectric

A. N. Nazarov[1], Y. V. Gomeniuk[1], Y. Y. Gomeniuk[1], V. S. Lysenko[1], H. D. B. Gottlob[2], M. Schmidt[2], M. C. Lemme[2], M. Czernohorsky[3], H. J. Osten[3]

[1] *V. E. Lashkaryov Institute of Semiconductor Physics, NASU, 03028 Kyiv, Ukraine*

[2] *Advanced Microelectronic Center Aachen, AMO GmbH, 52074 Aachen, Germany*

[3] *Institute of Electronic Materials and Devices, Leibniz University Hannover, 30167 Hannover, Germany*

Corresponding author. Phone +380445256262, Fax +380445256177, Email: yurigom@lab15.kiev.ua

Abstract. Charge trapping in ultrathin high-*k* Gd_2O_3 dielectric leading to appearance of hysteresis in *C–V* curves is studied by capacitance-voltage, conductance-frequency and current-voltage techniques at different temperatures. It was shown that the large leakage current at a negative gate voltage causes the reversible trapping of the positive charge in the dielectric layer, without electrical degradation of the dielectric and dielectric-semiconductor interface. The capture cross-sections of the hole traps are around 10^{-18} and 2×10^{-20} cm^2. The respective shift of the *C–V* curve correlates with a "plateau" at the capacitance corresponding to weak accumulation at the silicon interface.

Keywords: high-k dielectric, dielectric-semiconductor interface.

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1. Introduction

The dielectric materials with a high dielectric constant (high-*k* dielectrics) and metal gate electrodes are urgently needed to overcome the fundamental problems of silicon-based microelectronics on the way to progressively scaled node size. High-*k* dielectrics can be grown thicker than silicon oxide providing the same equivalent electrical oxide thickness (EOT) and offering significant gate leakage reduction due to suppressing the direct tunneling effects. Among high-*k* dielectrics, epitaxial rare earth oxides have been recently considered as perspective materials to replace silicon dioxide for future CMOS technology [1, 2].

At the same time, the problem of reliability and stability of new dielectrics still remains acute and requires further studies. Charge trapping in the dielectric layers of MOS transistors may be reversible, leading to the threshold voltage instability, and irreversible, changing the fixed charge concentration in the insulating layer. The latter effect affects the overall reliability of high-*k* structures reducing the carrier mobility in the channel in addition to permanent changes in threshold voltage thus causing the device operation failure. The former one is related to the threshold voltage instability which limits the operation speed [3]. Reversible charge trapping is usually detected as the hysteresis in capacitance – voltage (*C–V*) dependences of metal-insulator-semiconductor (MIS) capacitors measured at opposite directions of the voltage sweep. If application of negative or positive voltage leads to a persistent shift of the flat-band voltage, this is a sign of fixed charge trapping inside the insulating layer. Whereas the charge trapping in Hf-based dielectrics is studied thoroughly and the general understanding has been reached as to energy positions of related traps and to the physical nature of respective defects [4, 5], the Gd_2O_3 dielectric remains investigated much less.

In this letter, we report the results of investigation of unusual charge trapping phenomena in MIS capacitors with the novel material combination of epitaxial Gd_2O_3 high-*k* gate dielectrics and fully silicided NiSi gate electrodes on silicon substrate. This charge trapping results in hysteresis of *C–V* characteristic (reversible charge trapping) and occurs at such a high current density flowing through the structure, which usually causes irreversible charge trapping and degradation of the dielectric-semiconductor interface.

2. Experimental

Epitaxial Gd_2O_3 high-*k* dielectric layers have been grown on (001)-oriented *p*-silicon substrate (with the resistivity of 12–16 Ω/cm) by molecular beam epitaxy at 600ºC and covered *in vacuo* by a protective amorphous silicon layer. The physical thickness of Gd_2O_3 layer was 4.6 nm. Circular NiSi electrodes have been fabricated by

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full silicidation and reactive ion etching. The diameter of the metal dots was 0.3 and 0.4 mm. The details of sample preparation can be found elsewhere [6, 7].

The MOS capacitors were characterized by capacitance-voltage (*C–V*), conductance (*G–ω*), current-voltage and current-time measurements at different temperatures with an Agilent 4284 LCR meter and an Agilent 4156C semiconductor parameter analyzer.

3. Results and discussion

Fig. 1 shows the 1 MHz *C–V* curves measured at room temperature from accumulation to inversion and back. The large shift of *C–V* curves to the left may be caused by at least two reasons. The first one is the fixed positive charge inside the oxide layer. The second one is related to the large interface states density that could be expected in these samples, because no post-metallization forming gas annealing was performed. It was shown [8] that interface states densities of the order of 5×10^{12} $eV^{-1}cm^{-2}$ can shift the high-frequency *C–V* characteristic toward accumulation voltages by 1–2 V as compared to the low-frequency one. Our *G–ω* measurements give the value of interface state density near the valence band edge as high as 7.5×10^{12} $eV^{-1}cm^{-2}$.

An interesting feature is the kink in the lower part of the curves. It is definitely related to some recharging processes and not to the deep depletion effect, since the minimum capacitance C_{min} approaches a constant value near 0 V, and the calculation of the impurity concentration using this value of C_{min} gives more reasonable result (9×10^{14} cm^{-3}), than if the plateau value is taken instead of C_{min}. The calculation of the surface potential shows that the flat-band capacitance lies below the plateau value and the flat-band voltage is about –0.6 V (inversion at the semiconductor-dielectric interface starts at around –0.4 V). This means that the processes responsible for the plateau take place at weak accumulation at the silicon surface. The most intuitive would be to assign this kink to interface states localized in the narrow energy interval within the bandgap, as this was considered in the paper by Hurley *et al*. [9], where the *C–V* measurements were performed at a low frequency. However, several arguments can be adduced against of this for our high-frequency measurements. First, the interface states have to give equal contribution to the total capacitance for a given value of the voltage applied independently of the gate voltage sweep direction. In our case the height of the plateau is different for different directions of the sweep. Second, we have specially chosen a high measuring frequency to minimise the interface states contribution. At lower frequencies the hump is much more pronounced, but the difference between forward and reverse branches is still present. And third, the general features of the kink do not change with lowering the temperature (see Fig. 2), whereas for interface traps the respective peak vanishes with lowering the temperature [10]. Thus, we assume that the interface states in our measurements are not the main factor resulting in creation of the capacitance kink.

A strong hysteresis between forward and backward branches of *C–V* curve indicates that some recharging processes occur inside the dielectric also at the negative gate voltage corresponding to strong accumulation. If the *C–V* characteristic was measured starting from inversion to accumulation and back, the same hysteresis was recorded. To check the kinetics of this process, we recorded the *C–V* curves keeping the constant gate

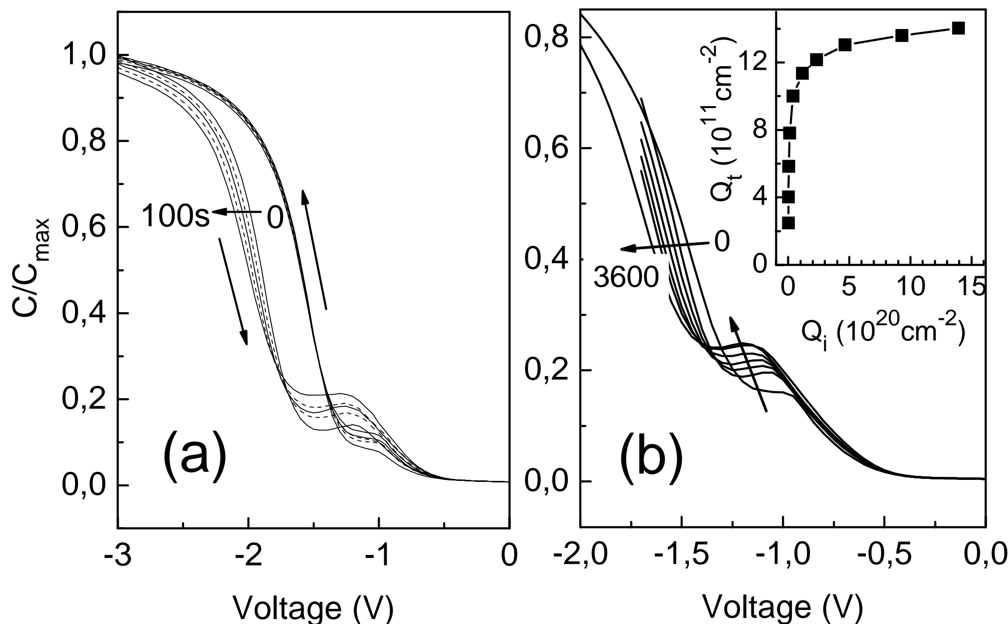

Fig. 1. (a) *C–V* characteristics at 300 K measured with hold times 0, 3, 10, 30 and 100 seconds at accumulation voltage -3 V. (b) *C–V* curves with holding at -1.7 V for 0, 3, 30, 300 and 3600 seconds. The *C–V* curve measured from 0 to -2.5 V and back is shown for reference. Inset shows the kinetics of charge trapping.

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voltage V_g=–3 V (Fig. 1a) and –1.7 V (Fig. 1b) for some holding time after turning the structure into accumulation. The increase of holding times leads to a gradual shift of *C–V* characteristics to more negative voltages which should be attributed to the positive charge trapping in the dielectric. At the same time, all backward sweeps practically coincide. If the measurements started from inversion, the holding at the corresponding voltage (0 V) did not result in any shift of both branches of the *C–V* curve.

The measurements with different holding time did not result in any irreversible changes of the *C–V* curve. After the series of negative bias stressing experiments the *C–V* characteristic with zero holding time was the same as the initial one except of some minor modification of the shape. This proves that the dielectric does not degrade after the application of negative voltage, no new traps are created within the insulating layer and at the Si/Gd_2O_3 interface, and the hysteresis is caused by reversible charge trapping at preexisting intrinsic traps.

To check the features of discharging the traps, we made several cycles of *C–V* measurements starting from strong accumulation to some point at the plateau and backward. Fig. 3 presents the respective *C–V* curves. Recharging the traps takes place mainly at the gate voltages corresponding to the plateau. The inset shows the amount of released charge in dependence on the gate voltage at which the sweep direction was changed. This is another indication that kinks on *C–V* curves are due to reversible charging and discharging of holes inside the insulator.

The kinetics of positive charge trapping calculated from the *C–V* curve shift after the negative voltage applied (V_g = –1.7 V) using the method suggested by Nazarov *et al.* [11] is presented in the inset of Fig. 1b. The value of injected charge was calculated by multiplying the forward current density at this voltage by the holding time. The estimations show that charging is related to two types of hole traps with the capture cross-sections of the order of 10^{-18} cm^2 and 2×10^{-20} cm^2. It should be noted that this is a lower estimate for the trap cross-section value, since the total current through the structure may include both hole and electron components whereas only the hole component is responsible for positive charge trapping. The absence of the *C–V* shift at backward sweeps means that the whole additional trapped positive charge in the dielectric is released completely at inversion condition at the Gd_2O_3-Si interface.

Fig. 2 shows the temperature dependences of the observed hysteresis. It can be seen that the hysteresis is more pronounced at higher temperatures. We relate this to the fact that in this case the current flowing through the structure is much higher (*J–V* temperature dependences are shown in Fig. 2c). Stretching the *C–V* characteristics with decreasing temperature is probably related to redistribution of the voltage across the structure and/or to additional charge trapping in the

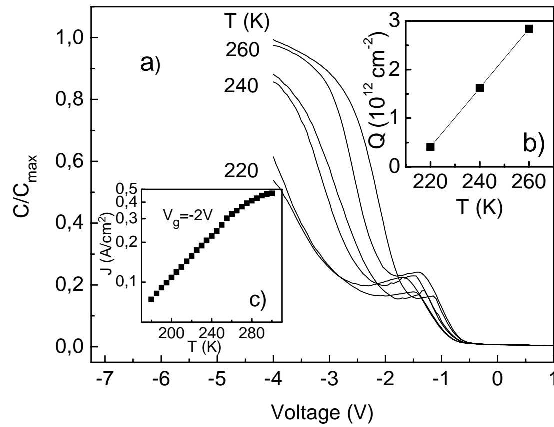

Fig. 2. (a) *C–V* curves at different temperatures. (b) Captured positive charge vs. temperature. (c) Temperature dependence of the forward current.

interface traps. At lower temperatures, the parasitic series resistance of the silicon substrate increases and becomes comparable to the resistance of the dielectric layer and, as a result, the effective gate voltage reduces by an amount of the voltage drop across the semiconductor bulk.

Based on the presented results, we can make a conclusion that the kink of the *C–V* curves observed in NiSi/Gd_2O_3/Si system is due to fast recharging of the hole traps located within a tunnel distance from the interface and energetically situated slightly below the top of the valence band. If we change the gate voltage from 0 V (inversion) to negative values, at some point the trap level aligns with the Fermi level (see Fig. 4a), then the hole traps start charging and until all the traps are filled the surface potential remains almost unchanged though the gate accumulation voltage increases. After filling these traps, the surface potential again follows the

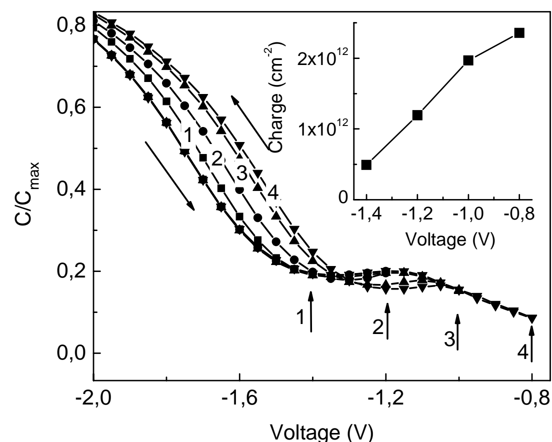

Fig. 3. Dependence of hysteresis on the voltage at which the sweep direction changes. Arrows indicate the return points for the *C–V* curves, backward branches of which are marked with respective numbers. Inset shows the amount of released charge in dependence of the return point position.

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gate voltage, and the surface is turned into strong accumulation. From the length of the plateau (along the voltage axis), one can evaluate the concentration of these traps (around 2.5×10^{12} cm^{-2} in our case). The energy position of the trap can be roughly estimated assuming that the voltage drop across the dielectric is linear. If the tunnel distance is about 1 nm and the valence band offset is equal to 2 eV [12], then the respective trap is located at 1.8 eV above the top of the Gd_2O_3 valence band.

At higher negative voltages, we observe trapping of additional positive charge at the traps with relatively small cross-sections. These traps could be the shallower hole traps in the Gd_2O_3 bandgap (1.2 eV above the valence band) which were suggested to be responsible for current transport through the dielectric film [12]. Filling these shallow traps modifies the band diagram in such a manner that the filled deep trap level responsible for the plateau moves down (see Fig. 4b). If then we sweep the gate voltage from accumulation to depletion, the charge release starts at the point where this level aligns with the Fermi level in semiconductor. This occurs at higher negative voltage than for depletion-accumulation sweep (see Fig. 4c), as observed in our experiments. During discharging the hole traps, the dynamic equilibrium exists between changing the gate voltage and the charge moving from the dielectric that results in interface potential stabilization. Thus, the length of the "plateau" during discharging allows us to estimate the total trapped charge in Gd_2O_3 located both at the tunnel distance from the interface and in the dielectric bulk. The maximum trapped positive charge can be estimated as 3.6×10^{12} cm^{-2}.

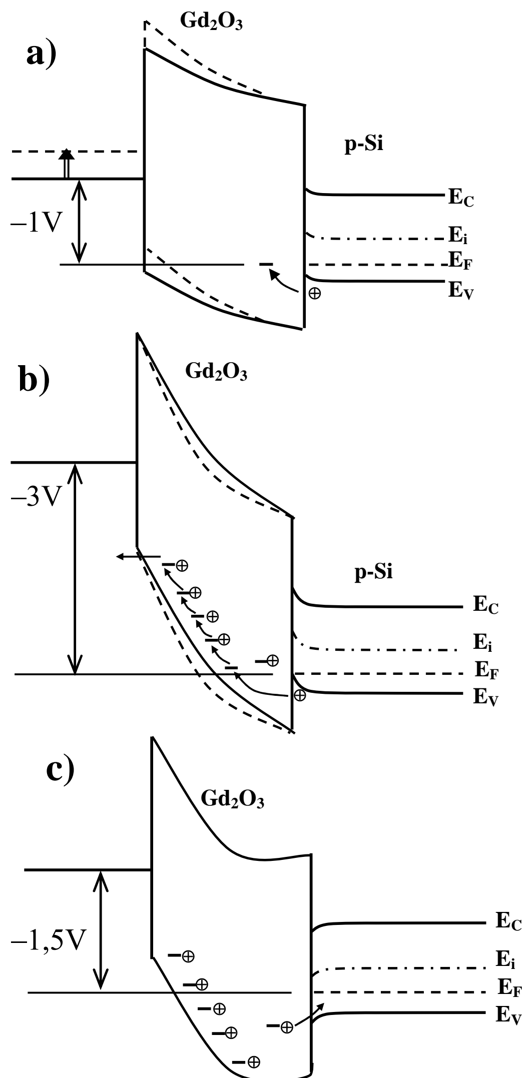

Fig. 4. Schematic energy band diagrams: (a) Filling the deep hole trap within the dielectric bandgap. (b) Filling the shallow hole traps when the accumulation voltage is kept for some holding time. Captured positive charge modifies the shape of the band edges as shown by dashed lines. (c) Release of the trapped positive charge during backward voltage sweep.

4. Conclusions

In this paper, the results of investigations of charge trapping in the MOS structures with new $NiSi/Gd_2O_3$ gate stack are presented. It was shown that in the accumulation mode the strong leakage current leads to charging of hole traps inside the dielectric. Turning the structure into inversion seems to discharge these traps completely. Three types of hole traps are responsible for the observed charging/discharging behaviour: one deep trap at the tunneling distance from the dielectric/semiconductor interface and two shallower traps with different cross-sections located inside the gadolinium oxide film. Large current densities flowing through Gd_2O_3 layer result in no degradation of the dielectric and/or interface quality.

5. Acknowledgements

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