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Low-frequency noise in nFinFETs of different dimensions processed in strained and non-strained SOI wafers

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Abstract. The results of low-frequency noise investigation in fully-depleted (FD) nFinFETs of W_{eff} = 0.02 to 9.87 μm, L_{eff} = 0.06 to 9.9 μm, processed on standard (SOI) and strained (sSOI) wafers are presented. It is shown that the McWhorter noise is typical at zero back gate voltage for the devices studied and the density of the corresponding noisy traps in the SiO_2 portion of the gate oxide is, as a rule, much higher than that in the HfO_2 portion. The results on the McWhorter noise are used for studying the behavior of the electron mobility μ and the free electron density N_S in the channel at $V^* \geq 0.4$ V where V^* is the gate overdrive voltage. It is also shown that the Linear Kink Effect (LKE) Lorentzians appear in the low-frequency noise spectra at an accumulation back gate voltage and that the parameters of those Lorentzians are different for the sSOI and SOI nFinFETs. This is the first observation of the LKE noise under a back-gate accumulation bias for sufficiently wide nMuGFET.

Keywords: low-frequency noise, FinFET, fully-depleted, SOI, sSOI, Linear Kink Effect.

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1. Introduction

In order to overcome the current limitations of traditional dimensional scaling, performance boosters like strain and multiple gate architectures are currently of strong interest. The combination of both by fabricating for example n-channel FinFETs on strained-Silicon-on-Insulator (sSOI) substrates may yield additional drive current improvement compared with standard SOI substrates. While this is aiming in the first place to digital applications, the question arises what the analog potential of such technologies is. An important aspect there is the low-frequency (LF) noise behavior. The fact that the sidewall channels are on (110) faces for a standard (100) SOI substrate raises concerns regarding a higher density of interface and bulk oxide traps, and, hence, the LF noise. Another concern may be the application of strain on the quality of the gate oxide/silicon interface, which can be addressed by noise measurements. It is the aim of the present work to investigate the noise in n-channel triple gate MuGFETs with a SiO_2/HfO_2/TiN gate stack, fabricated on sSOI and SOI substrates, as a function of the device dimensions and bias conditions. It is shown that for most devices studied, a higher trap density is derived in the vicinity of the SiO_2/HfO_2 interface compared with the bulk HfO_2. Only a minor impact of the strain has been noted. In addition and maybe more of academic value is the first observation of the Linear Kink Effect (LKE) noise under a back-gate accumulation bias for sufficiently wide nMuGFETs. In this case, a different behavior is found between SOI and sSOI devices.

2. Experimental

The investigated devices were n-channel fully-depleted (FD) FinFETs processed on both the standard (SOI) and strained (sSOI) SOI wafers. The parameters of the devices were as follows: h = 65 nm and 55 nm for SOI and sSOI nFinFETs, respectively, W_{eff} = 0.02 to 9.87 μm, L_{eff} = 0.06 to 9.9 m, where h is the fin height, W_{eff} and L_{eff} are the effective fin width and length, respectively. In the case of W_{eff} = 0.02 μm the multiple fin configuration was used where the fin number N_{fin} was equal to 30. The full device width Z has been calculated by the formula $Z = N_{fin} \cdot (2h + W_{eff})$. The gate stack consisted of 2 nm HfO_2 on the top of 1 nm interfacial SiO_2, so that one has for the equivalent oxide

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thickness: t_{EOT} = 1.9 nm. The gate electrode was 5 nm MOCVD TiN with a 100 nm poly-Si cap. No channel doping was used.

The drain current noise spectral density $S_I(f)$ within the frequency range f = 0.7 Hz to 100 kHz was measured on wafer at 0.3 V ≤ V_{GF} ≤ 1.6 V, and V_{DS} = 25 mV for V_{GB} = 0 (an accumulation back-gate voltage) where V_{GF}, V_{DS} and V_{GB} are the front gate, back gate and drain voltage, respectively.

3. Results and discussions

1. The families of the drain current noise spectra $S_I(f)$ measured at different V_{GF} and V_{GB} = 0 for the sSOI and relatively long SOI devices of W_{eff} = 0.02 µm are shown in Fig. 1. It is seen that for the SOI FinFETs the noise spectra are of the $1/f$ type up to sufficiently high frequencies where the $1/f$ component is lost in the Nyquist noise. It is also seen that for the sSOI FinFETs the $1/f$ portion of the noise spectra is observed only at f > 400 Hz while $S_I \sim (1/f)^{0.7}$ takes place at f < 400 Hz. Therefore, an essential difference in the shape of the noise spectra for the standard and strained devices of W_{eff} = 0.02 µm shows itself at f < 400 Hz. At the same time, it has been found that for the SOI FinFETs of W_{eff} ≥ 0.12 µm the spectra similar to those shown in Fig. 1b are typical. It should be noted that similar spectra are also observed for short (L_{eff} ≤ 0.16 µm) SOI devices of W_{eff} = 0.02 µm.

Fig. 2 demonstrates the dependences of S_I normalized for L_{eff} and Z on the gate overdrive voltage V^* measured at f = 3 kHz (curves 1 to 3) at which the $1/f$ noise prevails for both the sSOI and SOI FinFETs and at f = 10 Hz (curves 4 and 5) that corresponds to the $(1/f)^{0.7}$ noise. It is seen that S_I does not depend on V^* at V^* > (0.2–0.8) V for both the $1/f$ and $(1/f)^{0.7}$ noise components. It should be noted that such a behavior is typical for the low-frequency noise of the McWhorter type [1, 2].

It is known that the McWhorter model ascribes the noise to the fluctuations of the number of electrons in the channel accompanying the electron exchange between the channel and the slow traps located in the gate dielectric at various distances x from the Si/SiO_2 interface. If those traps are distributed homogeneously over x, the $1/f$ noise has to be observed. However, if the density of the noisy traps, N_{ot}, decreases with increasing x, the noise spectrum has to be of the $(1/f)^m$ shape where m < 1 [1, 3]. Then the dependences $S_I \sim (1/f)^{0.7}$ considered above and observed at f < 400 Hz can be explained by the decrease of N_{ot} with increasing x at $x > x_0$. The value of x_0 can be estimated using the formula $x_0 = \lambda \ln[(2\pi f_0 \tau_{min})^{-1}]$ where λ = 0.1 nm is the tunneling parameter, f_0 = 400 Hz and $\tau_{min} = 10^{-10}$ s [3], which gives x_0 = 1.5 nm. As to the $1/f$ noise showing itself at f > 400 Hz in the sSOI devices, this noise corresponds to the traps located at $x < x_0$, i.e. more close to the Si/SiO_2 interface.

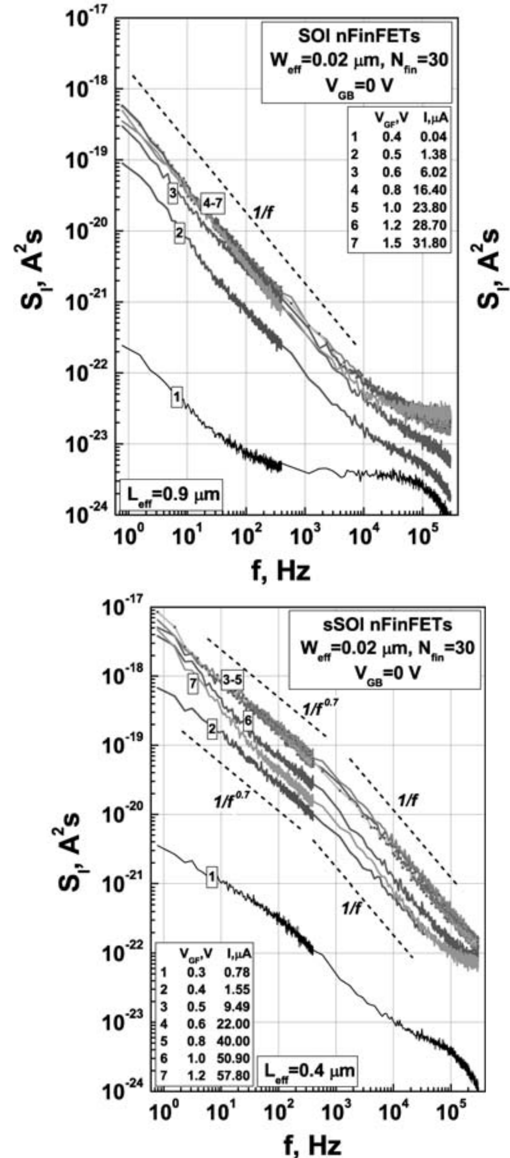

Fig. 1. Spectra of the drain current noise for the SOI (a) and sSOI (b) FD nFinFETs of W_{eff} = 0.02 µm measured at V_{GB} = 0.

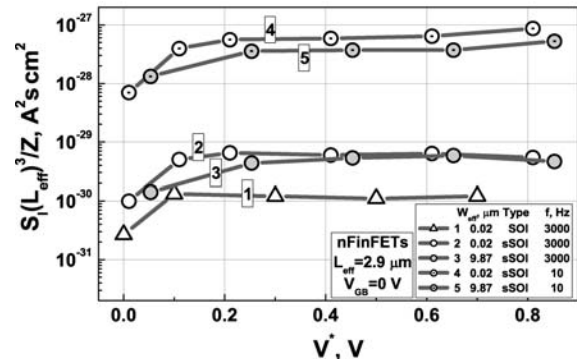

Fig. 2. Dependences of the drain current noise spectral density normalized for L_{eff} and Z on the gate overdrive voltage measured at f = 3 kHz (*1-3*) and 10 Hz (*4* and *5*) for SOI (*1*) and sSOI (*2-5*) nFinFETs of W_{eff} = 0.02 µm (*1*, *2* and *4*) and 9.87 µm (*3* and *5*); V_{GB} = 0.

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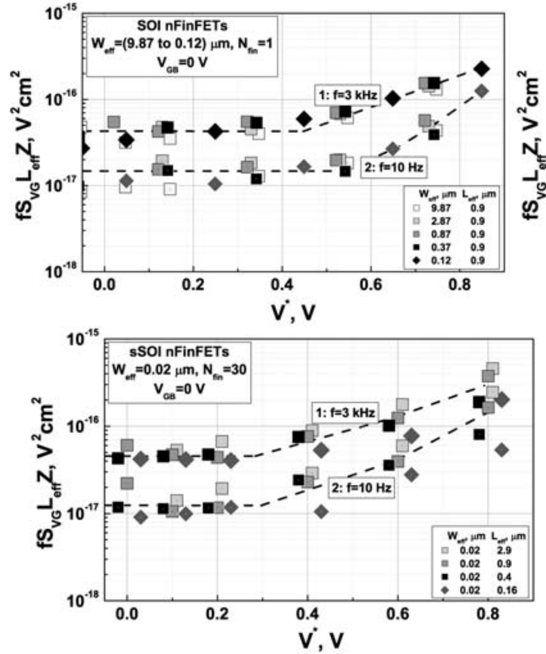

Fig. 3. Equivalent gate voltage noise normalized for $L_{\rm eff}$ and Z at different gate overdrive voltages for SOI nFinFETs of $W_{\rm eff}$ = (0.12–9.87) µm and $L_{\rm eff}$ = 0.9 µm (a) and sSOI nFinFETs of $W_{\rm eff}$ = 0.02 µm and $L_{\rm eff}$ = (0.16-2.9) µm (b) measured at f = 3 kHz (1) and 10 Hz (2); $V_{\rm GB}$ = 0.

The dependences of the value of $S_{\rm VG}L_{\rm eff}Z$ on V^* where $S_{\rm VG}$ is the spectral density of the equivalent gate voltage noise determined by $S_{\rm VG} = [S_I / (g_m)^2]$, where g_m is the transconductance are shown in Fig. 3. As is seen, the typical for the McWhorter noise plateaus where $S_{\rm VG}$ is independent of the gate overdrive voltage manifest themselves in the range $0 < V^* \le 0.4$ V for both $1/f$ noise (curve 1) and $(1/f)^{0.7}$ noise (curve 2).

Fig. 4 presents the values of $N_{\rm ot}$ calculated by the formula $N_{\rm ot} = (fS_{\rm VG}L_{\rm eff}ZC_0^2) / q^2kT\lambda$, where $S_{\rm VG}$ corresponds to the above mentioned plateau, C_0 is the capacitance of the gate oxide per cm^2, q is the electron charge, k is the Boltzmann constant and T is the temperature. The open circles and triangles in Fig. 4 correspond to the $1/f$ noise component and relate to the traps located at $x < x_0$ in the sSOI FinFETs and in the SOI ones of some dimensions ($W_{\rm eff}$ = 9.87 µm or $W_{\rm eff}$ = 0.02 µm and $L_{\rm eff}$ = 0.16 µm) as well as to the traps distributed homogeneously over x in the SOI FinFETs of $W_{\rm eff}$ = 0.02 µm and $L_{\rm eff}$ > 0.16 µm. The data shown in Fig. 4 by the dot center circles and triangles have been found by application of the formula $N_{\rm ot} = (fS_{\rm VG}L_{\rm eff}ZC_0^2) / q^2kT\lambda$ to the results measured for the $(1/f)^{0.7}$ noise at f = 10 Hz. Note that the frequency f = 10 Hz corresponds to x = 1.93 nm.

It is seen from Fig. 4 that $N_{\rm ot} = (2 \text{ to } 3)\times10^{19}$ cm^{-3}eV^{-1} at $x < x_0 \approx$ 1.5 nm while the lower values of $N_{\rm ot}$ [$N_{\rm ot} = (4 \text{ to } 8)\times10^{18}$ cm^{-3}eV^{-1}] have been found at $x > x_0$ for the sSOI devices and the SOI ones of $W_{\rm eff}$ = 9.87 µm. It is also seen that the values of $N_{\rm ot}$ responsible for both

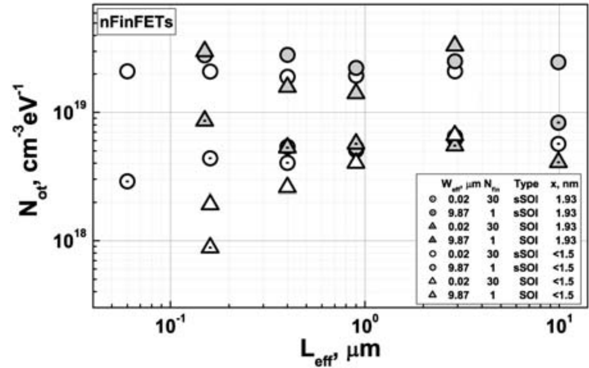

Fig. 4. Density of traps for SOI and sSOI nFinFETs of different $L_{\rm eff}$ and $W_{\rm eff}$ located in the gate oxide at various distances x from the SiO_2 interface.

the $1/f$ and $(1/f)^{0.7}$ noise in the devices of those types are practically independent of $W_{\rm eff}$ and $L_{\rm eff}$. It should be noted that the estimated value of x_0 (1.5 nm) is close to the thickness of the interfacial oxide layer (1 nm) used in the gate stack. This suggests that the traps characterized by the above mentioned higher density are located just in that oxide.

As to the SOI FinFETs of $W_{\rm eff}$ = 0.02 µm, it is seen from Fig. 4 that in the case where $L_{\rm eff}$ > 0.16 µm and the traps are distributed homogeneously over x, the value of $N_{\rm ot}$ decreases from 7×10^{18} cm^{-3}eV^{-1} to 3×10^{18} cm^{-3}eV^{-1} as far as $L_{\rm eff}$ decreases from 2.9 to 0.4 µm. It is also seen from Fig. 4 that in the case where $L_{\rm eff}$ = 0.16 µm and the values of $N_{\rm ot}$ are different at $x < x_0$ and $x > x_0$, they appear to be relatively low, namely: $N_{\rm ot} = 2\times10^{18}$ cm^{-3}eV^{-1} and $N_{\rm ot} = 9\times10^{17}$ cm^{-3}eV^{-1} for $x < x_0$ and $x > x_0$, respectively.

2. The obtained noise results can be used when considering the dimension behavior of the electron mobility µ as well as the behavior of the dependences $I(V^*)$ in the devices studied.

The values of μ_m corresponding to maximal values of the transconductance are shown in Fig. 5 for the devices of different types and dimensions. It is seen that: (i) μ_m decreases with decreasing $L_{\rm eff}$ (Fig. 5a); (ii) at not too small $L_{\rm eff}$ the values of μ_m for the sSOI devices are higher than those for SOI (Fig. 5a and b); (iii) μ_m increases with decreasing $W_{\rm eff}$ at $W_{\rm eff}$ > 0.9 µm and becomes practically independent of $W_{\rm eff}$ at $W_{\rm eff}$ < 0.9 µm (Fig. 5b). Note that the same features have been observed previously in the 65 nm FD planar SOI nMOSFETs [4].

It is known that the decrease of μ_m with decreasing $L_{\rm eff}$ can be connected with increasing $N_{\rm ot}$ [5]. The increase of $N_{\rm ot}$ with increasing $W_{\rm eff}$ could be also responsible for the corresponding decrease of μ_m. However, a comparison of Fig. 5 with Fig. 4 shows that there is no correlation between $\mu_m(L_{\rm eff}, W_{\rm eff})$ and $N_{\rm ot}(L_{\rm eff}, W_{\rm eff})$. Therefore, the dimension dependences of μ_m observed are not connected with the dimension dependences of $N_{\rm ot}$.

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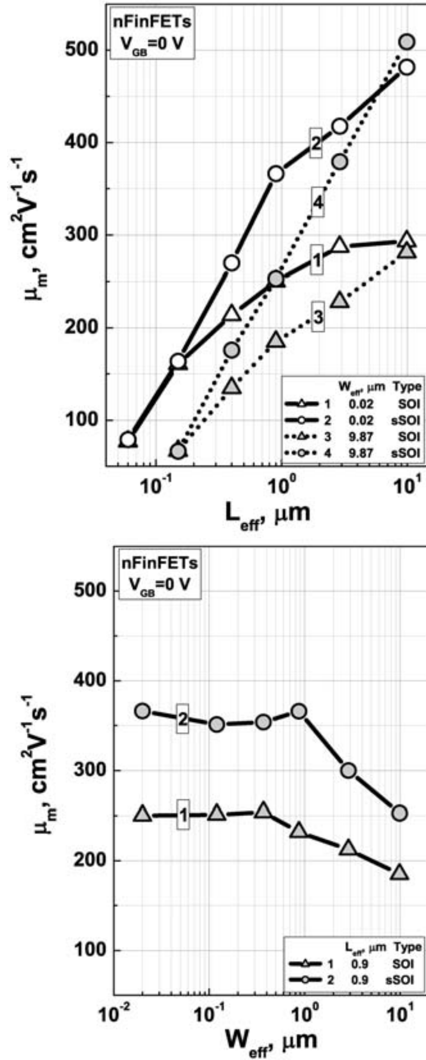

Fig. 5. Electron mobility corresponding to the maximum of the transconductance at different L_{eff} (a) for SOI (*1* and *3*) and sSOI (*2* and *4*) nFinFETs of $W_{eff} = 0.02$ μm (*1* and *2*) and 9.87 μm (*3* and *4*) and at various W_{eff} (b) for SOI (*1*) and sSOI (*2*) nFinFETs of $L_{eff} = 0.9$ μm; $V_{GB} = 0$.

It should be noted that the higher values of μ_m in FinFETs where $W_{eff} = 0.02$ μm $<< 2h$ than in FinFETs where $W_{eff} = 9.87$ m $>> 2h$ (Fig. 5a) can be explained by $\mu_{side} > \mu_{top}$ [6], where μ_{side} and μ_{top} are the values of μ_m for the sidewall and top portions of the channel. However, it has been found that $\mu_{side} < \mu_{top}$ for nFinFETs [7]. Moreover, the method proposed in [6] can be used only in the case where $\mu \neq \mu(W_{eff})$. At the same time, Fig. 5b demonstrates the increase of μ_m with decreasing W_{eff} at $W_{eff} > 0.9$ μm for the FinFETs, where $W_{eff} >> 2h$ and, hence, $\mu_m = \mu_{top}$. Therefore, like for the 65 nm FD planar SOI nMOSFETs [4], the increase of μ_{top} with decreasing W_{eff} takes place in the FinFETs considered. Then such an increase of μ_{top} at $W_{eff} < 0.9$ μm could be responsible for the higher values of μ_m in the FinFETs of $W_{eff} = 0.02$ μm even under conditions where $\mu_{side} < \mu_{top}$.

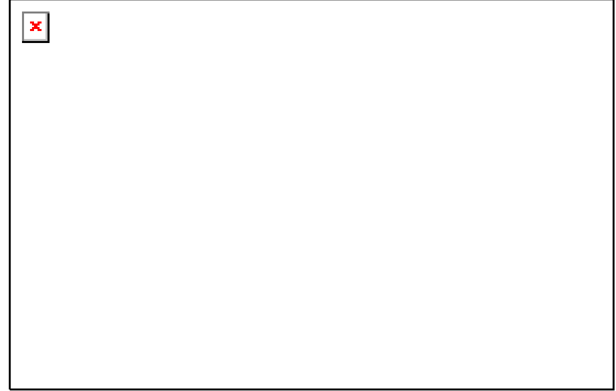

Fig. 6. Dependences of the drain current normalized for L_{eff} and Z on the gate overdrive voltage for sSOI FinFETs of $L_{eff} = 0.9$ μm and $W_{eff} = 0.02$ μm (*1*) and 9.87 μm (*2*) measured at $V_{GB} = 0$.

As to the behavior of I with V^*, it has been found that the increase of I with increasing V^* becomes sublinear at $V^* \geq 0.4$ V (Fig. 6) that is at rather low V^* where such an effect cannot be related to the influence of the series resistance and usually is attributed to the decrease of the electron mobility with increasing V^*. At the same time, our noise measurements have shown that $S_I \neq S_I(V^*)$ at $0.1\ \text{V} \leq V^* \leq 0.8$ V (Fig. 2). Since for the McWhorter noise $S_I \sim \mu^2$, this suggests that $\mu \neq \mu(V^*)$ in the above mentioned range of V^* and, hence, the sublinear behavior of $I(V^*)$ at $V^* \geq 0.4$ V is not explained by a decrease of μ. The possible reason for this effect is the sublinear increase of the free electron density in the channel N_S with increasing V^*. A similar situation has been observed previously for the planar nMOSFETs [2].

3. It has been found that under conditions where an accumulation voltage is applied to the back gate, the LKE Lorentzians [8] appear in the noise spectra measured at $1\ \text{V} \leq V_{GF} \leq 1.6$ V for the sSOI and SOI nFinFETs of $W_{eff} \geq 0.9$ μm (Fig. 7). It should be noted that this is the first observation of the LKE noise under a back-gate accumulation bias for sufficiently wide nMuGFETs. The behavior of the parameters of those LKE Lorentzians (the Lorentzian plateau $[S_I(0)]_{LKE}$ and time constant τ_{LKE}) are shown in Fig. 8. It is seen from Fig. 8a that $[S_I(0)]_{LKE} \sim \tau_{LKE}$ that is typical for the LKE Lorentzians [8] and that $\{[S_I(0)]_{LKE}/\tau_{LKE}\} \sim (L_{eff})^{-n}$ where $n < 3$ while $n = 3$ has been observed for planar MOSFETs with similar lengths as in Fig. 8a [8]. Since $[S_I(0)]_{LKE} \sim \mu^2$ [8], one of the reasons for this effect is the decrease of μ with decreasing L_{eff}.

As to the behavior of τ_{LKE} with V_{GF}, it is seen from Fig. 8b that: (i) the sSOI FinFETs are characterized by much higher values of τ_{LKE} at one and the same values of V_{GF}; (ii) $\tau_{LKE} \neq \tau_{LKE}$ (L_{eff}) at $L_{eff} \geq 0.9$ μm while the values of τ_{LKE} for $L_{eff} = 0.4$ μm appear to be lower than for $L_{eff} \geq 0.9$ μm, and this effect is more strong for the sSOI FinFETs than for the SOI ones. Since the considered LKE Lorentzians have been observed at

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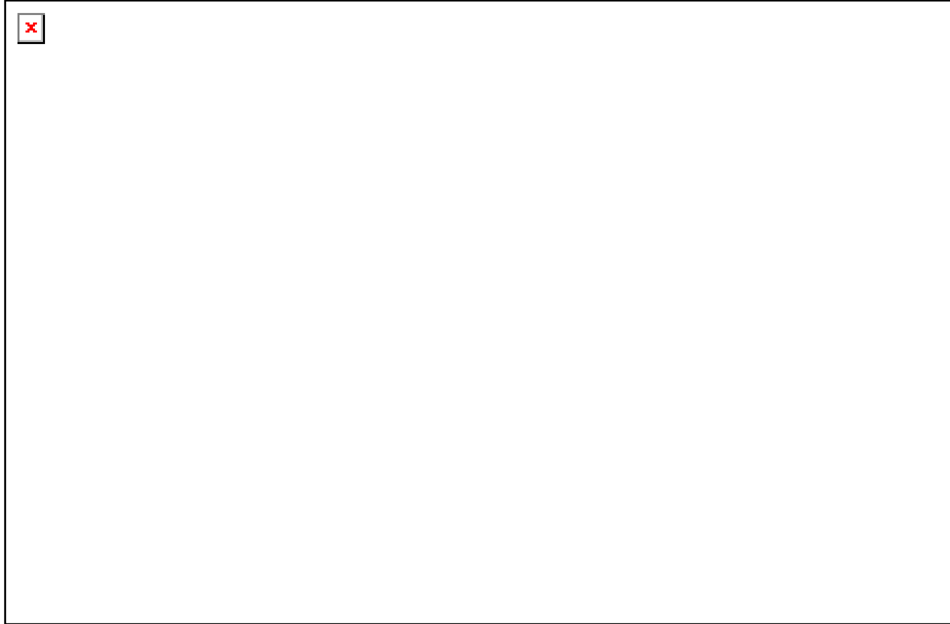

Fig. 7. Spectra of the drain current noise measured at accumulation back-gate voltage V_{GB} = –9.48 V for the SOI (a) and sSOI (b) FD nFinFETs of W_{eff} = 9.87 μm and L_{eff} = 0.9 μm.

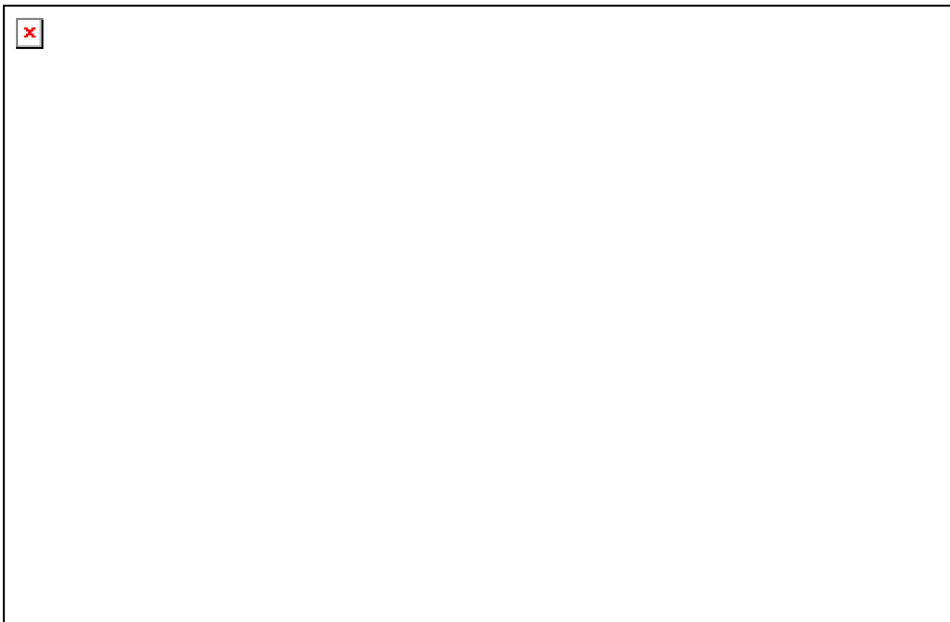

Fig. 8. Dependences of the LKE Lorentzian plateau on the time constant (a) and of the LKE Lorentzian time constant on the front gate voltage (b) measured at V_{GB} = –9.48 V for sSOI nFinFETs of W_{eff} = 9.87 μm and L_{eff} = 2.9 μm (1), 0.9 (2), and 0.4 (3).

$V^* < 1$ V, where the values of τ_{LKE} are determined by the electron valence band tunneling not only through the gate oxide but also through the silicon film depletion layer [9], this effect can be related with different conditions for such tunneling in sSOI and SOI FinFETs.

4. Conclusions

1. The low-frequency noise of the McWhorter type is typical at $V_{GB} = 0$ for the nFinFETs investigated. For the sSOI devices, the densities of the noisy traps located in the gate oxide at $x < 1.5$ nm and $x > 1.5$ nm, where x is the distance from the Si/SiO_2 interface into the oxide, are found to be N_{ot} = (2 to 3)×10^{19} $cm^{-3}eV^{-1}$ and N_{ot} = (4 to 8)×10^{18} $cm^{-3}eV^{-1}$, respectively, the values of N_{ot} are practically independent of W_{eff} and L_{eff}; for the SOI ones of W_{eff} = 0.02 μm, the values of N_{ot} appear to be lower.

2. The LKE Lorentzians have been revealed in the low-frequency noise spectra for the devices of $W_{eff} \geq 0.9$ μm at 1 V ≤ V_{GF} ≤ 1.6 V when measuring at an

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accumulation back-gate voltage, and the parameters of those Lorentzians are found to be different for the sSOI and SOI nFinFETs.

3. The results obtained for the McWhorter noise suggest that: (i) the dependences of μ_m and N_{ot} on the device dimensions do not correlate; (ii) the reason for the sublinear increase of I with increasing V_{GF} observed for the nFinFETs at $V^* \geq 0.4$ V is the sublinear increase of N_S but not the decrease of the electron mobility.

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