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Electrical activity of misfit dislocations in GaAs-based heterostructures

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Abstract. Electrical properties of lattice-mismatch induced defects in GaAs/InGaAs and GaAs/GaAsSb heterostructures have been studied by means of electron-beam induced current (EBIC) in a scanning electron microscope and deep-level transient spectroscopy (DLTS). DLTS measurements, carried out with *p-n* junctions formed near the heterostructure interfaces, revealed one electron trap and one hole trap induced by the lattice mismatch. The electron trap has been attributed to electron states associated with threading dislocations in the ternary compound close to the interface, whereas the hole trap has been ascribed to misfit dislocations at the heterostructure interface. Detailed investigation of the dependence of DLTS-line amplitude and its shape on the filling time of the traps with charge carriers allowed us to specify the type of electronic states related to both traps.

Keywords: semiconductor heterostructures, dislocations, deep levels, capture kinetics.

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1. Introduction

Lattice-mismatched GaAs-based heterostructures are of continual interest because of their application in high-speed and optoelectronic devices. Epitaxial growth of those heterostructures is accompanied by a strain in the epitaxial layer that results from a difference in lattice parameters between the substrate and the layer. If the thickness of the layer exceeds its critical value the strain is relieved by the formation of misfit dislocations. In heteroepitaxial semiconductor systems with zinc-blende structure and small lattice mismatch, grown on (001)-oriented substrates, orthogonal arrays of regular 60° misfit dislocations are formed at the interface [1]. The misfit dislocations are accompanied by threading dislocations which propagate into the epitaxial layer. Both kinds of dislocations can give rise to energy levels in the band gap which act as recombination centres or traps for free carriers and can lead to a degradation of the performance and reliability of heterostructure devices. Current requirements for device miniaturization make this detrimental activity of dislocations increasingly important. Because of translational symmetry along dislocation lines, one-dimensional energy bands rather than isolated localized electron states are expected to be associated with the dislocation cores.

In this report we present results of investigations of electrical properties of lattice-mismatch induced defects in GaAs-based heterostructures studied by means of electron-beam induced current (EBIC) in a scanning electron microscope and deep-level transient spectroscopy (DLTS).

2. Investigated heterostructures and EBIC characterization

We investigated two types of heterostructures, GaAs/InGaAs and GaAs/GaAsSb containing a small mole fraction, up to a few percent, of indium or antimony in the ternary compound, epitaxially grown on (001) oriented GaAs substrates. The first type structure was n^+-p heterojunction grown by molecular beam epitaxy (MBE) of InGaAs layer, with the In content of 3%, on n^+-type GaAs. The second type of structures were p^+-n heterojunctions fabricated by liquid-phase-epitaxy (LPE) growth of $GaAs_{1-x}Sb_x$ layers on p^+-type GaAs. Three structures with different Sb contents in the epilayer (x = 1, 2 and 3%) and, in addition, a reference heterostructure

without Sb were grown simultaneously to ensure the same growth conditions of the layers. In both cases the top layer was intentionally doped to form either n^+-p or p^+-n junction near the interface. The p-n junction was situated in the ternary-compound layer, shifted by a fraction of a micrometer with respect to the plane of the heterointerface [2].

A difference in lattice constant between GaAs and the ternary compound (about 0.2 % at 3 % of In or Sb content) resulted in generation of a two-dimensional network of misfit dislocations lying along two orthogonal <110> directions at the (001) interface. Such a dislocation network has been revealed with EBIC technique utilizing the p-n junction situated near the interface. It is shown in Fig. 1 where the misfit dislocations are visible as dark lines owing to enhanced recombination rate of electron-hole pairs generated by an electron beam [3].

3. DLTS results and discussion

The spectrum of lattice-mismatch induced defects in both types of structures has been studied by means of DLTS using p-n junctions formed in the epilayers. This allowed for investigation of both electron traps in the upper half of the band gap and hole traps in the lower half.

Only two deep-level traps, both related to lattice-mismatch induced defects, have been revealed in MBE-grown GaAs/InGaAs heterostructures; Fig. 2. However, each one could be revealed under different bias conditions. The same deep-level traps have been also revealed in LPE-grown GaAs/GaAsSb heterostructures but, in that case, DLTS spectra contained also other lines associated with point defects present in those structures [2, 4].

The electron trap, called ED1, has been revealed in the DLTS spectrum measured under typical bias conditions, i.e. under reverse quiescent bias, which was decreased to zero during the filling pulse. This trap has been attributed to threading dislocations in the layer of ternary compound close to the plane of p-n junction. The ED1 trap had been, for the first time, revealed by means of DLTS in plastically deformed bulk GaAs with a deep

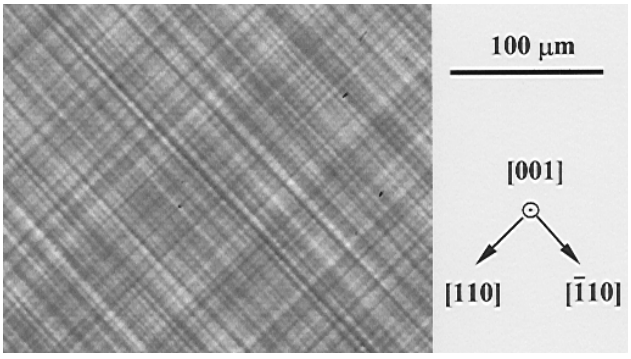

Fig. 1. Distribution of misfit dislocations at the interface of n^+-p GaAs/InGaAs heterojunction revealed by means of EBIC technique in a scanning electron microscope.

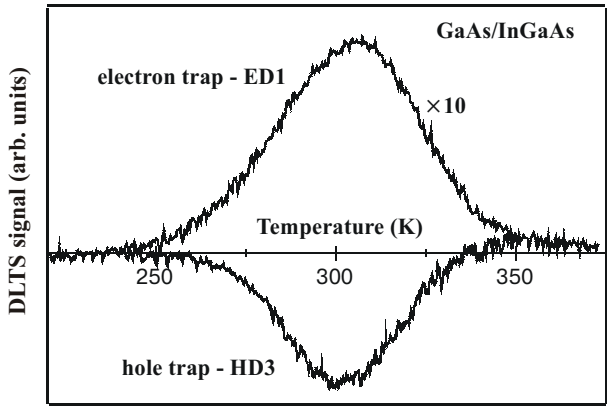

Fig. 2. DLTS spectra measured at a rate window of 48 s^{-1} for the n^+-p GaAs/InGaAs heterojunction. The upper spectrum was recorded under reverse-bias conditions while the lower one was detected under forward-bias injection.

level at E_C - 0.68 eV and related to electron states associated with 60° dislocations generated by plastic deformation [5].

DLTS measurements, carried out for GaAs/GaAsSb heterostructures with various Sb content, showed that the position of the ED1 line on the temperature scale shifted to lower temperature and its amplitude increased while the Sb-content in the ternary compound increased [4]. Fig. 3 presents the temperature dependence of the ther-

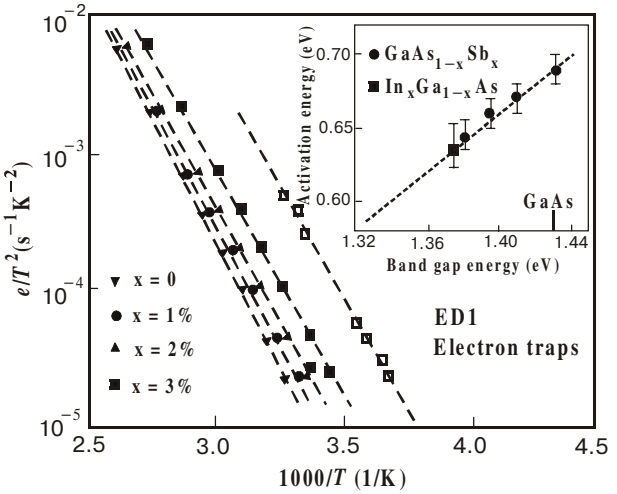

Fig. 3. Temperature dependence of the thermal emission rates (Arrhenius plots) for the ED1 electron trap revealed in the GaAs/$GaAs_{1-x}Sb_x$ heterostructures (full points) and GaAs/InGaAs heterostructure (open squares). Inset shows the electron-emission activation energy from ED1 traps versus band-gap energy at 300 K obtained for the GaAs/$GaAs_{1-x}Sb_x$ heterostructures (circles) and for the InGaAs/GaAs heterostructure (square). Broken line represents constant position of the trap level with respect to the valence-band edge of E_V + 0.74 eV.

mal emission rates of electrons from the ED1 trap (Arrhenius plots) measured by DLTS for both GaAs/GaAsSb and GaAs/InGaAs heterostructures. The activation energies of the ED1 trap, evaluated from the slopes of the Arrhenius plots, are shown in the inset. They decrease with an increase of the Sb or In content in the epilayer similarly to how the band-gap energy in the ternary compound decreases. This dependence indicates that the energy level position of the trap with respect to the top of the valence band remains the same in each material, suggesting that the defect state is composed primarily of the valence band states. Similar dependence can be also concluded from several DLTS studies of GaAs/InGaAs heterostructures with higher (6–30 %) In mole fractions [6-8].

Our DLTS measurements performed for the GaAs/InGaAs heterostructure under injection conditions, i.e. under zero quiescent voltage and forward-bias filling pulse, revealed one hole trap (Fig. 2), called HD3, with a deep level at $E_V + 0.67$ eV. We revealed the same hole trap in the DLTS spectra of GaAs/GaAsSb heterostructures, measured under forward-bias injection, however, the precise evaluation of the HD3 activation energy was strongly disturbed in that case owing to the position of its DLTS line on the high-temperature slope of another line associated with point defects present in those heterostructures [2]. In contrast to the ED1 trap, the DLTS line of the HD3 trap did not shift on the temperature scale while changing the Sb-content in the GaAs/GaAsSb heterostructures, but its amplitude increased with the increase of Sb-content. Fig. 4 presents the Arrhenius plots for the HD3 trap measured by DLTS in both types of structures. We relate the trap, which has been detected only when the DLTS-active region comprises the interface, to defects associated with the lattice-mismatched interface, most probably to misfit dislocations lying at the interface. Probably the hole trap recently found by Du et al. [9] in lattice-mismatched GaAs/InGaAs heterostructures with various In mole fractions and layer thicknesses is the same as HD3. That trap, labelled H4 by the authors, with the DLTS activation energy between 0.67 and 0.73 eV, has been related to misfit dislocations at the interface by comparing the DLTS spectra in various heterostructures with the distribution of dislocations revealed by means of transmission electron microscopy.

The principal argument for the assignment of the traps to dislocations was logarithmic kinetics for capture of charge carriers into the trap states. Such a kinetics results from the Coulomb interaction between a charge carrier just being captured and other charges already captured at the dislocation line [10]. This interaction manifests itself in DLTS measurements in a linear dependence of the signal amplitude on the logarithm of the filling-pulse duration [5], as shown for the ED1 and HD3 traps over several orders of magnitude of that duration; inset in Fig. 4. In contrast, isolated point defects or impurities exhibit exponential capture kinetics.

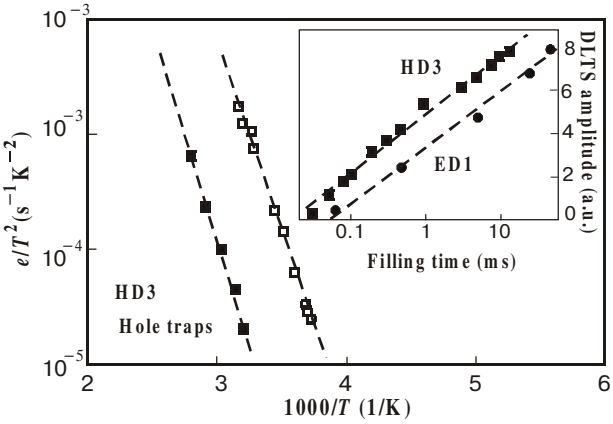

Fig. 4. Temperature dependence of the thermal emission rates (Arrhenius plots) for the HD3 hole trap revealed in the GaAs/$GaAs_{0.97}Sb_{0.03}$ heterostructure (full squares) and GaAs/InGaAs heterostructure (open squares). Inset shows DLTS-line amplitudes of ED1 and HD3 traps versus filling-pulse duration measured for the GaAs/InGaAs heterostructure.

Recently, Schröter et al. [11, 12] proposed a model of electronic states associated with extended defects in semiconductors. The authors proposed that their electronic states, forming an energy band, can be classified as *localized* or *bandlike* by taking into account the rate R_i, at which the states reach their internal electron equilibrium within the band. This internal equilibration rate, when compared to the carrier emission rate from the defect R_e and the capture rate R_c, allows us to distinguish between *localized* states ($R_i << R_e, R_c$) and *bandlike* ones ($R_i >> R_e, R_c$). The authors demonstrated, by computer simulation of DLTS spectra induced by the two types of states, that the states can be distinguished on the grounds of dependence of their DLTS-line shape on the filling-pulse duration.

For *localized* states the DLTS-line maximum stays constant while changing the filling-pulse duration, whereas the line amplitude exhibits a linear dependence on the logarithm of the filling time. Such behaviour we have actually found for the ED1 trap, as shown in Fig. 5 (left). Similarly, it was shown that the DLTS signal associated with 60° dislocations in plastically deformed Si can be described by this type of electronic states [11]. On the contrary, in the case of *bandlike* states, variation of filling-pulse duration results in broadened DLTS lines whose maximum shifts towards lower temperature with increasing that duration and whose high-temperature sides coincide. This is the case of the HD3 trap as demonstrated in Fig. 5 (right). Possibly, the electronic states associated with misfit dislocations belong to *bandlike* states because of a higher regularity of those dislocations as compared with the threading ones. To this category of states belong also electronic states associated with dislocation rings bounding nanoscale $NiSi_2$ precipitates in silicon [12].

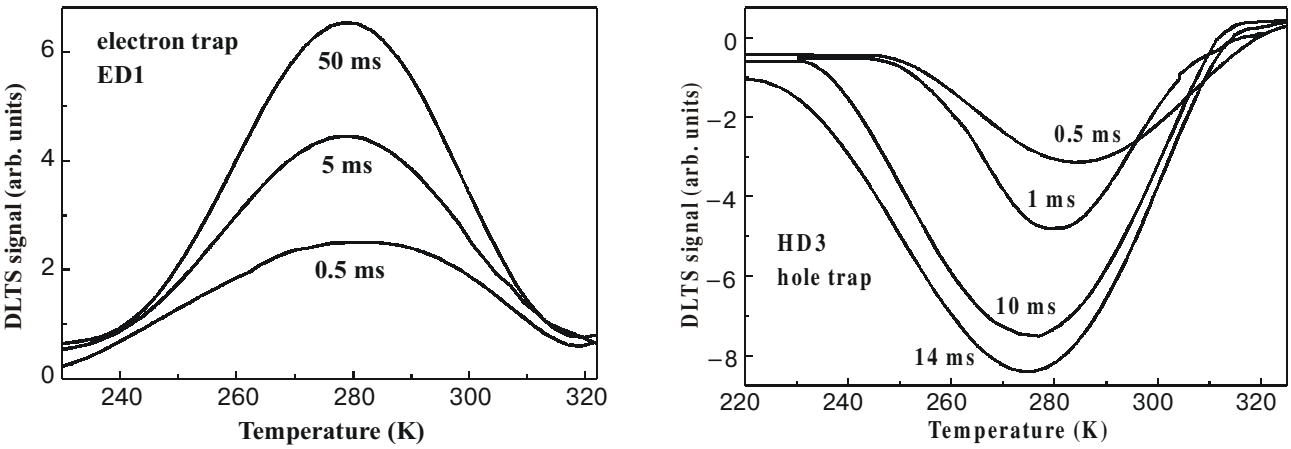

Fig. 5. DLTS lines of the ED1 trap (left) and the HD3 trap (right) and their dependence on filling-pulse duration, whose values are written in the figures, measured for the GaAs/InGaAs heterostructure at a rate window of 2 s^{-1}.

4. Conclusions

One electron trap and one hole trap have been found with the DLTS technique in lattice-mismatched GaAs/InGaAs and GaAs/GaAsSb heterostructures. The electron trap, called ED1, has been attributed to threading dislocations in the layer of ternary compound, whereas the hole trap, HD3, detected only when the DLTS-active region comprises the interface, has been related to misfit dislocations lying at the heterostructure interface. A thorough analysis of the dependence of DLTS-line amplitude and its shape on the filling time allowed us to specify the type of electronic states related to both traps. In terms of the model of electronic states associated with extended defects, which takes into account the rate at which the states reach their internal electron equilibrium, we relate the ED1 electron trap to *localized* states and the HD3 hole trap to *bandlike* ones.

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