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Silicon-on-insulator technology for microelectromechanical applications

A. Y. Usenko, W. N. Carr
New Jersey Microsystems, Inc.
240 King Blvd., Newark, NJ 07102, njm@technologist.com

Abstract. A purpose of the paper is to give a review of recent development (1998-1999) in microelectromechanical (MEMS) devices formed on silicon-on-insulator (SOI) substrates. Advantages of using SOI are summarised. Problems of CMOS-MEMS integration for smart sensors are listed. Examples of successful use of SOI to fabricate advanced MEMS are given and future prospects MEMS on SOI are evaluated.

Keywords: micromechanical systems, silicon-on-insulator, sensors, review.

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SOI is an extremely versatile starting material for fabricating micromechanical systems both with and without the inclusion of silicon integrated circuits on a shared substrate. SOI permits a means of structuring starting sandwich materials to provide a highly precise control of several material parameters in addition to permitting unique structures not easy to obtain without SOI technology. The SOI technology referred to in this paper extends beyond using silicon oxide as the dielectric to include customized dielectrics and substrates. We use this broad definition of SOI because that is precisely the direction that this technology will evolve as CMOS and bipolar integrated circuits are mated with MEMS in cost-effective and technology-enhanced ways.

The utilization of SOI for MEMS applications is summarized in the Table with respect to SOI structure and resulting advantages of performance, parameter specification, and processing. This summary does not permit detailing each structure since there are a large number of detail structures that will evolve from the marriage of MEMS with SOI technology.

A fundamental advantage of the SOI structure is that a thin surface film is obtained in which the film can be tailored by preprocessing of the source wafer to provide a precise film thickness, modulus, and doping properties. The SOI technology permits tailoring mechanical properties in addition to electrical properties in a very uniform manner. This basic process point provides a fundamental advantage to the use of SOI starting material in MEMS applications. In MEMS, warping of released structures is often a major problem especially when the released structure is of large area and thin. If thermistors or heating elements are incorporated into the released structure the advantage of using a bulk-derived film provides an important increase of uniformity in resistivity and resulting production yield.

For bimorph and multimorph surface structures the single, uniform film underlying CVD, evaporated, epitaxial, etc. films contributes to the overall uniformity of mechanical and electrical characteristics of the completed sensor or actuator structure. The increased tensile breaking (and plastic deformation threshold) of single crystal films invariably exhibit increased mechanical strength in a finished structure. Many flexed MEMS structures are improved by using films of increased tensile breaking stress.

The mechanical and electrical isolation that can be obtained by etching from either the topside or the back-

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Table. SOI-MEMS technology utilization summary.

SOI Structure	Performance	Parameter	Process
Released monomorph micro platform, cantilevers, beams as structural members, sensors, and actuators	More precise fabrication control	Reduced warping, controlled resistivity, uniform thickness, minimal internal stress, increased tensile breaking stress	Ease of film release The bonding dielectric becomes the sacrificial layer.
Released bimorph actuators and sensors	More narrow windows for sensitivities and actuation efficiency	Precision thickness, repeatable internal stress, higher deflection limits	Reduced yield spread requirement for deposited films
Internal dielectric etch stop	More narrow performance window	Precise control of semiconductor film thickness used with backside/frontside etching	Convenient etch stop for TMAH, EDP, KOH
Integrated circuits with MEMS on the same substrate	Higher speed, reduced spurious signal pickup, higher sensitivity	Reduced circuit capacitance, reduced magnetic pickup area, higher functional density	SOI is basically compatible with MEMS
Surface films customized using FZ, compensated CZ, and other preprocesses	Unique performance sensors	Unique parameters tailored for optical and IR elements, magnetometers, PIN diodes, bolometers	Obtainable only with SOI-type processing in many cases
Customized dielectrics instead of SiO_2	Tailoring of the dielectric constant and optical bandpass, for example	Control dielectric loss vector, permittivity, optical and IR index, thermal conductivity	Utilizes developed wafer bonding equipment
Customized substrates	Mechanical strength, optical transparency, thickness and thermal conductivity. Relates to packaging importantly	Control Young's modulus, permittivity, tensile breaking stress	Generally does not complicate processing

side of SOI wafers permits a variety of structures in which the dimensions can be precisely controlled. These dimensions are precisely controlled vertically by using the dielectric film within the SOI sandwich as an etch stop. In these processing situations the silicon is removed using a timed RIE process step or any combination of variety of anisotropic etchants including KOH, TMAH, EDP, and XeF_6.

The integration of CMOS and bipolar circuits onto a shared substrate with MEMS is the subject of considerable efforts worldwide. Using SOI an added opportunity exists to process CMOS or MEMS prior to SOI wafer bonding to obtain certain performance advantages. Most methodologies have resulted in integrated circuits being fabricated first where MEMS processing is a final process sequence with the release of MEMS structures.

When surface films of SOI starting materials are used as sensors it is possible to obtain an order of magnitude improvement in uniformity over deposited films. The uniformity advantage becomes even more important for large arrays fabricated using SOI structures. A similar customization can be obtained by selecting dielectrics other than SiO_2 as the dielectric sandwich materials. The dielectric can be tailored with a low dielectric constant to obtain improved performance of strip transmission lines in millimeter wave network applications, for example.

Examples of successful MEMS with SOI

Wafer bonding allows a new degree of freedom in design and fabrication of SOI material combinations [1,2,3] that previously would have been excluded because these material combinations cannot be realized by the conventional approach of epitaxial growth.

In [4] an SOI-based microelectromechanical quartz rate sensor is presented. These techniques have been adapted to applications in the aerospace, military, industrial, medical, telecommunications and automotive industries to realize miniaturized highly integrated MEMS in a cost-effective manner.

Studies on SiO_2-SiO_2 bonding with a hydrofluoric acid

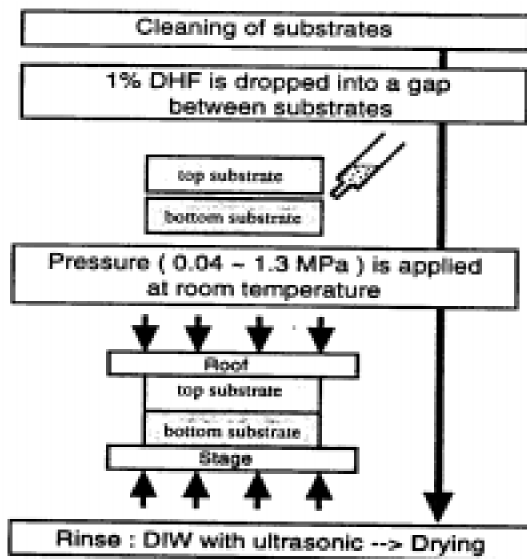


Fig. 1. Procedure of low temperature bonding for MEMS packaging [5].

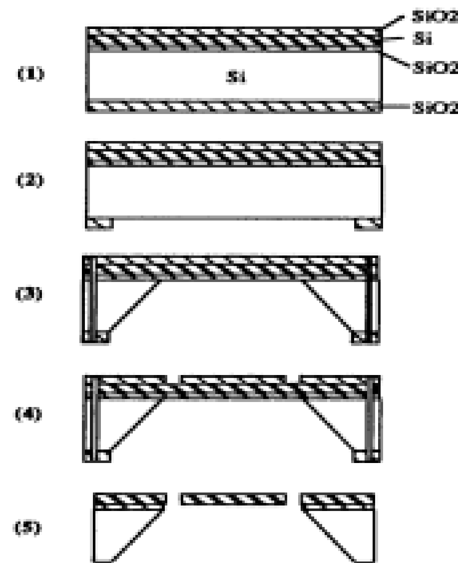


Fig. 2. Silicon micro-mirror fabrication process on SOI [9].

(HF) treated surface in [5] show a remarkable feature that bonding can be obtained at room temperature. Advantages of this method are low thermal damage, low residual stress and simplicity of the bonding process, which are expected for the packaging and assembly of MEMS, Fig. 1.

MEMS can build unique 3-D structures for critical RF (radiofrequency) components, such as suspended spiral inductors and intelligent microswitches/duplexers [6].

A simple technology for bulk-micromachined accelerometers [7] based on bond and etch back silicon on insulator (BESOI) wafers is described. This technology is an easy combination of bulk- and surface-micromachining technology using the buried oxide as a sacrificial layer allowing a precise control of the thickness of the beams and the fabrication of complex structures. Cantilever-beam, quad-beam, twin-mass and a new triaxial accelerometer have been fabricated and their results are described. Over-range structures have been included without any additional process step. The devices are anodically bonded to a glass wafer in order to reduce the package stresses and to control the damping of the structures.

A CMOS integrated [8] surface-micromachined angular rate sensor utilizing an electroformed vibrating metal ring structure on a silicon IC has been developed using SOI. Substantial signal-conditioning circuitry is included on the IC with the vibrating structure.

An asymmetric **micro-mirror** excited by an external piezoelectric ceramic vibrating element [9] directs an optical beam at an over-30-degree beam-scanning angle, Fig. 2. Using an SOI process simplifies the fabrication process and results in a very flat mirror surface. A structure consisting of two such mirrors (one horizontal and one vertical) was used to reproduce half-VGA computer images. Full displays should be possible by adding simple signal processing.

A silicon on insulator **pressure sensor** with enhanced performance [10] has been developed for use at very high temperatures. A Diffusion Enhanced Fusion (DEF) bonding technique has been employed for the formation of SOI wafers. This technique simultaneously allows for the bonding of sensing gages to the dielectrically isolated silicon diaphragm and for the improvement in mechanical electrical performance of the bonded sensor. The following improvements are obtained:

1) reduced thermal shift (1-2 mV over the temperature range from 420°C to 3700°C).

2) better thermal stability attributed to close thermal matching of the gages to the underling diaphragm (mechanical and electrical stability).

3) better passivation for high temperature operability. The SOI sensor structure obtained through DEF bonding approaches the optimum that can be achieved for a high temperature piezoresistive silicon pressure sensor.

A high temperature **pressure sensor** has been developed for measuring the cylinder pressure in combustion engines of automobiles [11]. The sensor is made of a membrane based piezoresistive β-SiC-on-SOI (SiCOI) sensor chip and a specially designed housing. The sensitivity of the sensor at room temperature is approximately 0.19 mV/bar and decreases to about 0.12 mV/bar at 300 °C.

Mirrors and **micromirror arrays** [12] made of monocrystalline silicon are described. Electrostatically operated two-directionally deflecting mirrors and mirror arrays

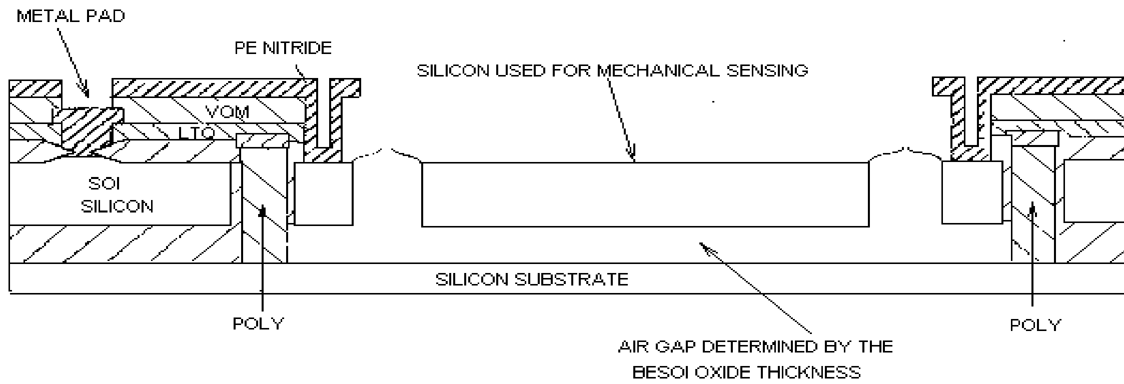


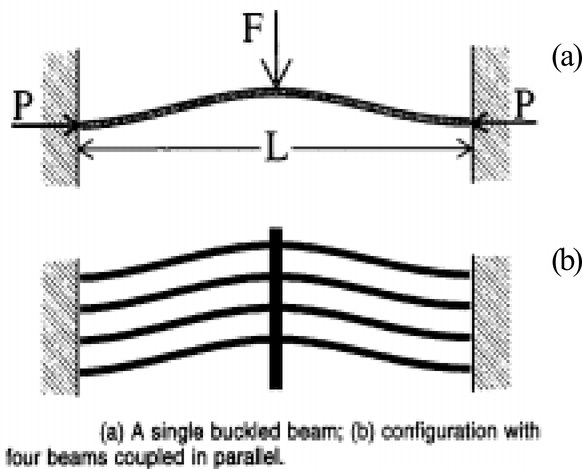
Fig. 3. Simplified cross-section of microaccelerometer on SOI [14].

for continuous scanning with working frequencies between several 100 Hz and 200 kHz are presented. The modified BESOI technology used and the experimental-data-based method to improve the accuracy of model parameters for simulations and to determine the cross-coupling between array cells are new in the field of micromechanics.

Accurate thermal simulations of SOI transistors and **cantilever** MEMS structures are described in [13] where lateral thermal conduction in the silicon device layer is determined by MEMS. The thermal conductivity decreases with decreasing layer thickness, d_s, to a value nearly 40 percent less than that of bulk silicon for d_s = 0.42 µm. The data show that the buried oxide in BESOI wafers has a thermal conductivity that is nearly equal to that of bulk fused quartz.

A surface micromachined **accelerometer** using SOI [14] is described, Fig. 3. Both the acceleration (or deceleration) sensor and associated signal conditioning circuitry are monolithically fabricated on the same substrate. The top silicon layer of the SOI wafer is the movable, common electrode of a differential capacitor pair. The components of the signal conditioning circuitry are fabricated in the SOI layer. The top silicon layer is single crystal silicon and does not suffer from the stress-related warping so common with polysilicon.

Micromachined, thermally insensitive **silicon resonators** with accuracy equivalent or superior to that of quartz resonators are fabricated from a micromechanical SOI process in [15]. A resonator forms a tuning fork gyroscope. Radiation-hard precision voltage references are made using the silicon resonators. Thermal stability is comparable to that of a quartz oscillator. By employing a micromechanical device based in a tuning fork gyro-



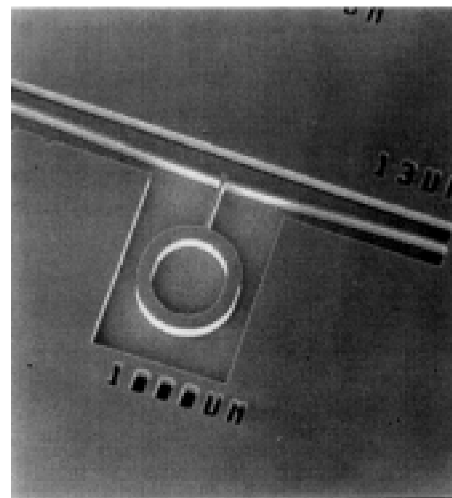


Fig. 4. Bistable buckled beam, its cross-section (left) and photograph (right) [16].

scope, resonators are made for either or both of the gyro drive and sense axes.

A lateral symmetrical **bistable buckled beam** for snap-in holding structures is a SOI structure described in [16], Fig. 4. The structures were fabricated by deep silicon reactive ion etching using the black silicon method than subsequently released and thermally oxidized. The bistability was monitored in situ in a scanning electron microscope using a micromanipulator.

KOH solutions for etching **extremely sharp silicon tips** on SOI is described in [17]. Etching of (100) silicon on SOI wafers was carried out over a wide range of reaction temperatures and KOH concentrations. The sharpness increases with temperature to a critical point and then decreases at very high temperature and KOH concentration. Hydrogen bubbles formed during etching are very important in determining both etch rate and sharpness of the tips. The sharpest tip dimension was found to occur at 30 % KOH and 70 °C reaction temperature.

A process for further reducing dimensions to a nanometer-scale for SOI MEMS has been demonstrated in [18]. Substrates was patterned using high resolution electron beam lithography with 100 keV electrons followed by Al evaporation and liftoff. The Al is used as an etch mask in CF_4 reactive ion etching to pattern the top silicon layer. Then structures were undercut using a buffered oxide etch. The structures were made from substrates having a top silicon thickness of 200 or 50 nm, and a buried oxide thickness of 400 nm. With this process a variety of movable structures have been made. The performance of an electrostatically driven **FabryPerot interferometer** that consists of a м sized platform suspended by wires that are 100-200 nm wide is described. Much smaller mechanical structures such as suspended silicon beams as narrow as 30 nm have also been made.

A new form of rotating media **disk drive** is described [19] using extremely sharp silicon tips. Data storage densities of many gigabits per square inch can be obtained. Data is stored in localized regions of electric charge that are stored within a thin dielectric layer that is coated upon both sides of an electrically conductive platter, rather than in magnetic domains. Data is read and written via ungated field emitter tips rather than with transformers and magnetically sensitive elements. The read/write head is built from the read/write head chip that contains field emitter tips and other elements. This chip is an active CMOS or other circuit whose active area is parallel to one side of a platter, rather than having a single, passive write element and a single, passive read element with external control circuits and amplifiers. The read/write head is a CMOS SOI with the tips and other microelectromechanical elements being formed in the top, silicon membrane, on isolated islands or pillars, and the supporting circuitry being formed in the base silicon wafer. Each read/write head chip is attached to the end of the arm of an actuator, in a manner similar to that used in magnetic disk drives.

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