Semiconductor Physics, Quantum Electronics & Optoelectronics, 2010. V. 13, N 1. P. 12-18

PACS 73.61.Cw, Ng

Electrical properties of semiconductor structures with Si nanoclusters in SiO_2 grown by high temperature annealing technology of SiO_X layer, X<2

S.V. Bunak, A.A. Buyanin, V.V. Ilchenko, V.V. Marin, V.P. Melnik*, I.M. Khacevich*, O.V. Tretyak, A.G. Shkavro
Taras Shevchenko Kyiv National University, Faculty of Radiophysics
64, Volodymyrska str., 01601 Kyiv, Ukraine
**V. Lashkaryov Institute of Semiconductor Physics, NAS of Ukraine*
41, prospect Nauky, 03028 Kyiv, Ukraine
E-mail: ilch@univ.kiev.ua

Abstract. The theoretical and experimental investigations of electrical properties of the SiO_2/Si-ncs/SiO_2/Si structures grown by high temperature annealing SiO_X, X<2, have been carried out. The influence of Si cluster growth conditions on frequency dependences of $C-V$ characteristics, static and dynamic conductance of investigated structures has been clearly observed. As a result of theoretical modeling, $C-V$ dependences have been calculated. The experimentally obtained negative constituent of differential capacitance has been qualitatively described. It has been experimentally found that the SiO_2/Si-ncs/SiO_2/Si structures with the tunnel dielectric layer revealed the effect of memorizing.

Keywords: nanocluster, static conductance, dynamic conductance, negative differential capacitance, memorizing effect.

Manuscript received 25.06.09; accepted for publication 22.10.09; published online 04.12.09.

1. Introduction

In recent years, structures of Si nanoclusters (Si-ncs), grown inside SiO_2 using different technological methods, attracts great attention of scientists because of possible prospects to create functionally new devices of nanoelectronics on their basis [1-3]. When studying the structures SiO_2/Si-ncs/SiO_2/Si formed by ion implantation of Si into SiO_2, memory effect [4] and light emitting diodes (LED) [5] were successfully obtained. There are cases of analogous structures obtained by high temperature annealing that reforms SiO_X layers, X<2, described in literature [6].

These technologies have some advantages in regard to compatibility with standard Si technology. This is one of the reasons that high temperature annealing is considered as the actual and perspective method for the future.

In the most papers, where luminescence in the structures SiO_2/Si-ncs/SiO_2/Si were studied, the main attention was paid to the influence of quantum-sized level of Si nanoclusters on the appearance of electroluminescence in the high-energy (blue or ultraviolet) part of the spectrum [7, 8]. At the same time, quantum states that always appear at the interfaces between Si and SiO_2, and energy levels related with existence of separate superfluous Si atoms in SiO_2 were devoted relatively few attention. In the meantime, it is well-known from the papers about kinetic processes of creation of Si nanoclusters in SiO_2 [9, 10] that structure always goes through the certain state with inner extraction of Si from SiO_X, X<2, in the course of annealing. The relatively larger quantity of Si, than it is necessary for the stoichiometric phase of SiO_2, is able to cause the formation of superfluous Si atoms and appearance of Si nanoclusters. The speed of migration process of Si atoms in a dielectric substantially influences on the process of formation of the interface states between Si nanoclusters and SiO_2 and on the formation of the separate inserts of Si atoms in SiO_2 that does possible forming the plural inserts of separate Si atoms in a SiO_2 matrix [3, 9].

The main task of this paper was to investigate electrical properties of the SiO_2/Si-ncs/SiO_2/Si structures grown by high temperature annealing SiO_X, X<2. With this purpose, it was theoretically and experimentally investigated the influence of quantum states formed in these structures during their annealing on temperature

and frequency dependences of $C-V$ characteristics, static and dynamic conductance of the SiO_2/Si-ncs/SiO_2/Si structures.

2. Experimental results and discussion

In this work, two types of structures were investigated. The structures of the first type were Schottky structures with thick enough (~800 Å) dielectric layer SiO_2 with Si nanoclusters. The structures of the second type were distinguished from first type by the existence of an additional 4.7-nm thick dielectric layer between Si and SiO_X. The additional dielectric layer was created due to dry thermal oxidation process in the initial Si substrate before deposition of SiO_X layer. As it will be shown below (see part 2.2), the existence of dry silicon dioxide layer made very essential influence on electrical properties of these structures and cause the appearance of memory effects on the structures of the second type. SiO_X films were deposited using universal vacuum assembly intended for the production of films from different materials by the methods of electron-beam and resistive evaporation. SiO_X films were deposited by the method of resistive evaporation of SiO powder from a Ta container. The temperature of evaporator was 1000-1200 ºC. Then, Si nanoclusters were formed using high temperature annealing in nitrogen atmosphere at 1100 ºC for 10 min. After structure formation, the Al contacts were created by the method of thermal evaporation.

2.1. The investigation of the structures without additional dielectric layer

Our experimental investigations were made using a computer-aided assembly for the measurements of static and dynamic conductivity and capacitance for various frequencies of the testing signal. For these purposes, we used picoamperemeter Keithley 6485 (the range of measured currents was from ±0.01 pA up to ±21 mA), LCR measuring device E7-12 and admittance measuring device INSTEK LCR-817. Both of measuring devices were able to apply external offset direct voltage from the source controlled by computer in the wide range of their values. The amplitude of the testing signal remained constant (20 mV) for all the measurements with different signal frequencies. All the temperature measurements were carried out in flowing nitrogen cryogenic temperature stabilization system with accuracy not worse than 0.1 ºC.

2.1.1. The investigation of capacitance of the structures without any additional dielectric layer

It is well-known [11-15] that charge accumulation and emission processes related to capture and escape of electrons are able to make very material effect on transport and capacitance properties of semiconductor structures with various nanoobjects, such as quantum dots or atomic clusters. Such kind of mechanisms is especially well investigated for the metal-GaAs structures with InAs quantum dots. The appearance of specific area with negative components on $C-V$ characteristics for these structures was described in detail in the literature [12-15]. This effect was clearly experimentally observed for the metal-GaAs structures with several layers of InAs quantum dots placed in the space-charge region of a Schottky diode. The main reason of this effect consists in the dynamic recharging of quantum dots due to capture and escape of electrons at a relatively low frequency of the testing signal. The decrease in the differential capacitance begins at the moment when imref crosses the energy level of quantum dots at some applied external voltage. In relation with this, on the usually monotonic $C-V$ curves a quite symmetric maximum could be clear observed, which is obtained at relatively low (0.3–10 kHz) frequencies.

Quite similar effect with a negative component of differential capacitance appears on $C-V$ curve for the SiO_2/Si-ncs/SiO_2/Si structures studied in this work for the 0.5–2 kHz frequency of the testing signal. At the same time, it is necessary to note that the area of capacitance maximum for these samples looks more asymmetric with long "tail" pulled out to the region of reverse biases.

The typical $C-V$ curve taken for the structures SiO_2/Si-ncs/SiO_2/Si at various frequencies of the testing signal is depicted in Fig. 1.

Being based on the results of $C-V$ measurements shown in Fig. 1, we determined the energy position of quantum states responsible for the accumulation of the charge in dielectric appearing additionally in the course of nanocluster growth by using the well-known admittance spectroscopy (AS) methods. It is possible to determine the values of capacitance that correspond to positions of peaks on $C-V$ curves measured at various temperatures (see Fig. 2). After that, determined using the standard methods was the activation energy of the quantum states responsible for the charge accumulation in dielectric from the slope of the Arrhenius plot. As this

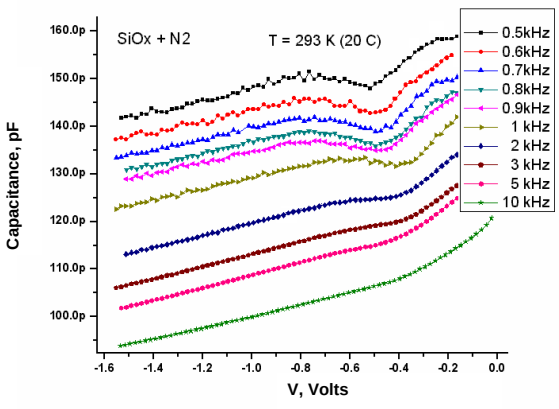

Fig. 1. $C-V$ characteristics of the structure without a tunnel dielectric layer at various frequencies of the testing signal at 293 K.

charge actually stipulated the frequency dependence of differential capacitance in the investigated structures, the activation energy for these levels was calculated by correlation substantiated in papers [14, 15].

2.1.2. Static and dynamic conductance investigation in SiO_2/Si-ncs/SiO_2/Si structures without additional dielectric

The processes of silicon extraction and migration are increased in the investigated structures as a result of increasing the annealing temperature and annealing time [3, 9]. Therewith, silicon atoms extraction occurs simultaneously over the thickness of initial SiO_X. Thereby, it is obligatory for such structure to be in certain state during the process of thermal phase transformation, when not all the excess silicon atoms, which would be released from oxygen bonds, will be a part of Si nanoclusters.

In the course of annealing, there are two competitive processes occuring in the structure: one part of Si atoms is directly used for creation of the clusters, while the other part forms a set of separate Si atom inclusions, which may be similar to the state of amorphous Si and can provide a fundamental possibility of electrical current flowing through the entire structure.

Depending on the technological parameters during annealing, the specific shares of Si atoms participating in these two processes can change, thus impacting on the Si clusters size and on properties of cross-cluster amorphous Si array built-in SiO_2, which in turn significantly influence on capacitance and transport characteristics of these structures.

As it can be seen from the graphs given in Fig. 3, the absolute value of the dynamic conductance, measured at the frequency 10 kHz, more than 10 times exceeds static conductance for the same samples.

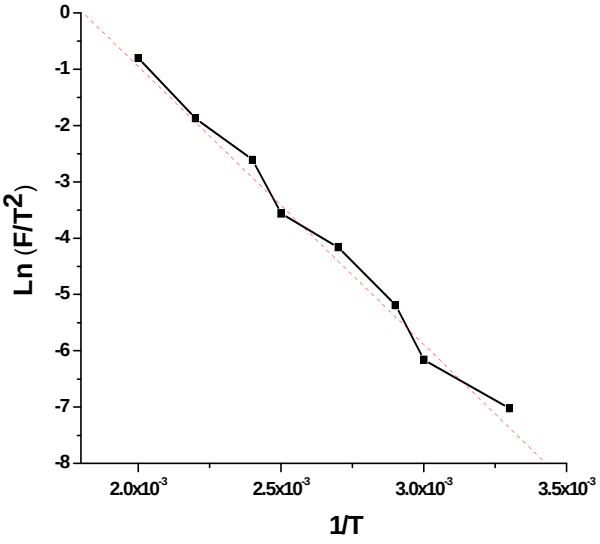

Fig. 2. Arrhenius plot for determination of the activation energy for trap levels.

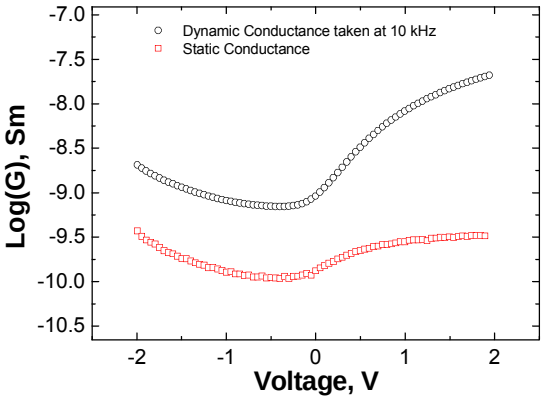

Fig. 3. Dependence of dynamic and static conductances on voltage for the structure without any additional dielectric layer.

On the assumption that the dynamic conductance can be associated only with the local percolation currents in the thick dielectric layer, one can conclude that for a low amplitude test signal (~20 mV), with which differential and dynamic capacitance were measured, there are only bias currents exist in the investigated structures. As for transport currents that pass through the entire structure at a constant applied voltage – they are much lower.

This explanation correlates well with the idea that quantum states involved in the electric charge accumulation process are galvanically connected with each other due to the existence of grid of closely located nanoclusters and due to separate Si atom inclusions, which makes the specific conductance to be connected with hop transport mechanism of charge carriers [6, 9, 10].

Assuming that the grid of individual Si atom inclusions represents bound percolation cluster that is formed in the entire dielectric layer, it should be expected that $I-V$ curves for such structures should be similar to those of a-Si/c-Si heterostructure. Temperature dependence investigation of $I-V$ characteristics measured at constant voltage makes it possible to determine the activation energy of conduction currents. It is close to $E_a = 0.3$ eV. $I-V$ curves for these structures showed a non-linear dependence on voltage, although the rectifying effect was very small. $I-V$ curve obtained and its temperature dependence were quite similar to those previously described in the works where analyzed are electrical properties of a-Si/c-Si heterostructures. The activation energy determined from experiments correlates well with energy parameters defined in [16, 17] for the a-Si/c-Si interface. This fact gives reasons to believe that the current passing in the grid of separate Si atom inclusions in SiO_2 occurs by the same (hopping) mechanism as in amorphous Si. It should be emphasized that the conductivity dependence on the applied voltage frequency is typical for hop conductivity mechanism in "density-of-states tails" in amorphous semiconductors [18]. Thus, the resulting

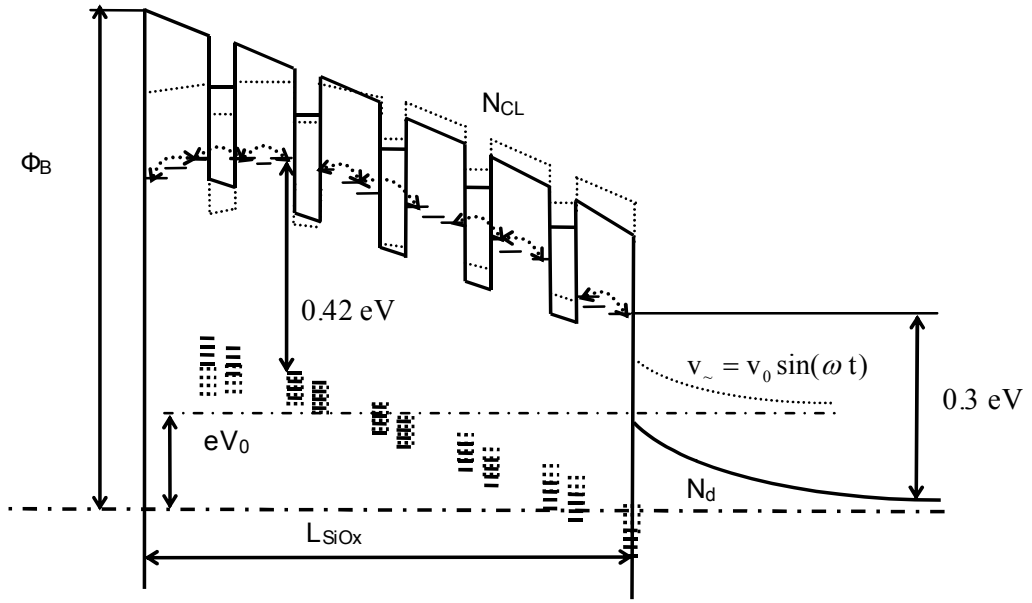

Fig. 4. Schematic band diagram of the potential profile for the SiO_2/Si-ncs/SiO_2/Si structure.

currents through the entire structure are determined by the conductivity in the "narrow" places in the percolation cluster of the separate Si atom inclusion grid. At the same time, the conductivity of alternating currents is determined by local characteristics of separate areas, where the coherence of nanoclusters grid and separate Si atom inclusions is relatively higher.

The experiments carried out allow to draw the conclusion that one can observe three different types of quantum levels in SiO_2/Si-ncs/SiO_2/Si structures, and their distribution by energy and concentration can significantly affect electrical and optical properties of these structures. They are: quantum-dimensional levels of nanoclusters, interface quantum levels formed at boundaries between Si clusters and the surrounding SiO_2, as well as quantum levels belonging to the grid of separate Si atom inclusions. The latter can conduct the current, which is rather unusual for a thick (~800 Å) silicon oxide. The obtained values of activation energies determined experimentally were used to build a physical model of SiO_2/Si-ncs/SiO_2/Si structure, band diagram of which is shown in Fig. 4.

2.1.3. Modeling the capacitance-voltage characteristics for SiO_2/Si-ncs/SiO_2/Si structures without any additional dielectric layer

Changing the charge on the quantum levels in thick dielectric when changing the test signal frequency gives a possibility to understand the origination mechanism of the negative differential capacitance effect in such structures, which is typical for these objects.

This simulation was carried out under the assumption that the spatial distribution of charge accumulated on quantum levels in this dielectric has been placed as layers at equal distances from each other (Fig. 4). This idealization was used only for discretization of the problem.

The calculation technique of frequency dependences for the capacitance was previously described in [15], so in this paper we have described only concept description of the problem and analysis of the obtained results. During the calculation, it was taken into account that the charge accumulated at the interface level can influence on the potential barrier profile in dielectric, which should significantly affect the magnitude of the differential capacitance of the structure. Since relaxation of the charge captured on the interface levels has certain characteristic times, it is completely natural that its frequency dependence takes place. In addition, our calculations show that the magnitude of this charge may be so considerable that it could exceed the total integrated amount of the charge in the space charge region of semiconductor, which in turn can cause the change of electric field direction inside the dielectric.

Fig. 5 shows the theoretical curve of capacitance-voltage dependence, which was obtained by modeling the structure with the dielectric thickness 210 nm, for seven cluster layers with the quantum level energy position close to 0.4 eV, which was counted from a certain energy level typical for the states in the grid of separate Si atom inclusions, through which hop transport of charges occurs over the whole structure.

The calculations carried out agree well with the results of experimental studies and make it possible to explain the appearance of the $C-V$ peak with its quite wide half-width and specific dependence "tail" tightened in the area of reverse voltages.

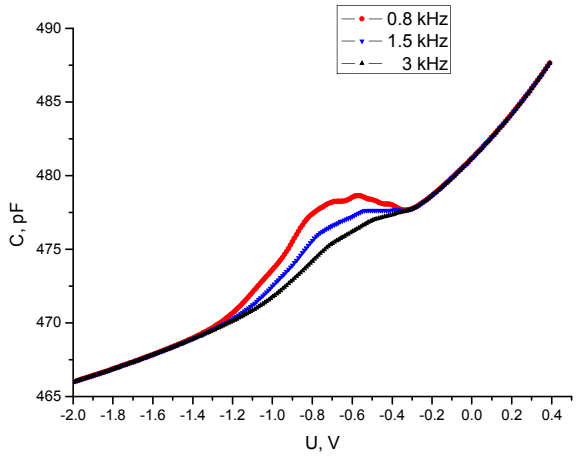

Fig. 5. The result of modeling the $C-V$ characteristic of SiO_2/Si-ncs/SiO_2/Si structure for 7 layers of quantum states with the activation energy level 0.4 eV.

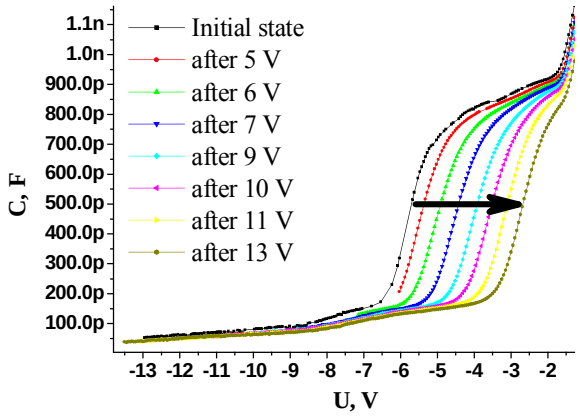

Fig. 6. $C-V$ characteristics of the structure with tunnel dielectric after the application of a considerable reverse bias (shift of $C-V$ characteristics is related to memorizing process).

Since contribution of the quantum states to capacitance increases slightly with the reverse voltage increase, the capacitance reduces in the reverse branch of $C-V$ characteristics not so rapidly as in the classic MIS structures. That's why, in our view, the "long tail" in the characteristic depending on $C-V$ curve maximum tightened in the area of reverse voltages has been observed in experimental $C-V$ curves.

2.2. The investigation results of structures with a tunnel dielectric layer

It should be noted that for the structures with a thin (~ 4.7 nm) dielectric layer thermally generated on the silicon substrate before SiO_X layer deposition, $C-V$ frequency dependences inherent to structures without any tunnel dielectric layer were completely absent. Instead of it, when increasing the reverse voltage applied to the structure, a gradual CVC shift to the right along the abscissa axis, where voltage values are marked, was observed (see Fig. 6).

It means that in the process of applying a certain reverse bias to the structure, the dielectric region begins to charge. It means accumulation of charge in it, which already cannot be changed quickly.

As the transport of charge is practically halted in these structures, then it is natural to do an assumption that an accumulation of charge occurs on the quantized levels of the interface states near nanoclusters, as their density of states substantially exceeds the density of the quantum-dimensional states of nanoclusters.

The amount of charge accumulated in the interface states is gradually increased with increasing the voltage. The process of charging the structure becomes considerable when the voltage equals to 5 V and reaches its maximum at 13 V. The same effect can be attained by applying short pulses of voltage of the same amplitude to this structure [19].

In the absence of the voltage applied to the structure, with the lapse of time there is a gradual shift of $C-V$ characteristic to the left along the voltage axis. It means that there is gradual discharging the reservoirs for accumulation of charge, related to the nanoclusters, as a result of thermal generation of charge carriers from quantum levels.

The dynamics of this process is presented in Fig. 7 for a several time values and room (297 K) temperatures. The process of thermal discharging is considerably more long as compared with the process of charging and with a time of measuring the $C-V$ curve, that is, actually, enables to observe it. The complete discharging of the structure takes place at room temperature approximately for three days.

On the basis of aforesaid, it is possible to draw a conclusion that the investigated structure can be successfully used for the creation of dynamic memory device. It is necessary also to take into account a circumstance that the accumulation of charge in these structures allows to substantially decrease the sizes of modern memory devices compared with the sizes of structures created using the effect of charging the "floating gate". In addition, as defects in a dielectric layer cannot influence on discharging of the interface states near all the nanoclusters simultaneously, these structures must be more reliable.

It is separately needed to notice that in the processes of charging (accumulation of charge) and discharging, the investigated structures demonstrate a behavior conceptually very similar to that of self-assembled quantum dots. The interface quantum states round the Si nanoclusters that can accumulate a considerable electric charge in itself, like to quantum dots, are, in fact, zero-dimensional objects where motion of electrons is bounded in all three dimensions. A main difference between these objects consists of that for the

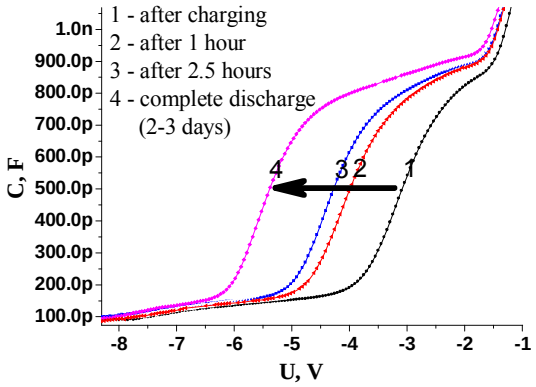

Fig. 7. The dynamics of discharging process in the structure with a thin tunnel dielectric layer (recovery of $C-V$ characteristics of structure with time at room temperature 293 K).

structures of SiO_2/Si-ncs/SiO_2/Si the quantum states, where an accumulation of charge is, are in considerably more wide bandgap material. Therefore, characteristic times of recharge become considerably longer (~10^1 hours).

3. Conclusions

Being based on our analysis of the experimental data, it is possible to draw the following conclusions.

The view of $C-V$ characteristics of the SiO_2/Si-ncs/SiO_2/Si structure, measured at low frequencies (~10 kHz) of the test signal, is similar to $C-V$ characteristics of the Schottky barrier structures based on GaAs with a several layers of InAs self-assembled quantum dots. It has been experimentally found that for the SiO_2/Si-ncs/SiO_2/Si structures with Si-nanoclusters without a tunnel dielectric layer an area with a negative differential capacitance is also present in $C-V$ dependences for low frequencies of measurements. The effect of negative differential capacitance component for these structures is expressly observed at room temperatures within the range of frequencies from 0.5 to 15 kHz when measuring the capacitance. Using the Arrhenius method, the activation energy of quantum levels was determined. These quantum levels, by their physical nature, probably arise up on interfaces between Si-nanoclusters and SiO_2.

As a result of modeling the $C-V$ characteristics, $C-V$ dependences are calculated, which qualitatively describe appearance of an area with the negative constituent of differential capacitance on them, because of the influence of interface states that arise between nanoclusters and dielectric.

It has been experimentally found that the SiO_2/Si-ncs/SiO_2/Si structures with the tunnel dielectric demonstrate the effect of memorizing. The technological conditions of production of Si-nanoclusters in the SiO_2/Si-ncs/SiO_2/Si structures with a tunnel dielectric are found ($T_{anneal.}$ = 1100 °C, t = 10 min), at which these structures demonstrate aforesaid memorizing properties. Characteristic voltages of charging (~10 V) and characteristic times of discharging (~50 hours) are determined for such structures at room temperatures. It is assumed that using these structures as memory devices will allow decreasing the size of storage elements to the size of a several Si-nanoclusters (~20-30 nm).

References

1. V.N. Bogomolov, V.G. Golubev, N.A. Feoktistov, A production of regular three-dimensional lattices of silicic clusters of submicron sizes in SiO_2 matrix // *Zhurnal Tekhnicheskoy Fiziki* **24** (8), p. 90-95 (1998), in Russian.
2. I. Crupi, D. Corso, G. Ammendola, S. Lombardo, C. Geradi, B. DeSalvo, G. Ghibaudo, E. Rimini, and M. Melanotte, Peculiar aspects of nanocrystal memory cells: Data and extrapolations // *IEEE Trans. Nanotechnology* **2** (4), p. 319-323 (2003).
3. G.A. Kachurin, V.A. Volodin, D.I. Tetelbaum, D.V. Marin, A.F. Leier, A.K. Gutakovsky, A.G. Cherkov, A.N. Mikhailov, Formation of silicon nanocrystals in SiO_2 layers by implantation of Si ions with intermediate annealing // *Fizika Tekhnika Poluprovodnikov* **39** (5), p. 582-586 (2005), in Russian.
4. C. Bonafos, M. Carrada, N. Cherkashin, H. Coffin, D. Chassing, G. Ben Assayag, A. Claverie, T. Müller, K.H. Heinig, M. Parego, M. Fanciulli, P. Dimitrakis, P. Normand, Manipulation of two-dimensional arrays of Si nanocrystals embedded in thin SiO_2 layers by low energy ion implantation // *J. Appl. Phys.* **95** (10), p. 5696-5702 (2004).
5. P.T. Huy, V.V. Thu, N.D. Chien, C.A.J. Ammerlaan and J. Weber, Structural and optical properties of Si-nanoclusters embedded in silicon dioxide // *Physica B: Condensed Matter*. **376-377**, p. 868-871 (2006).
6. S. Oda, Charge storage in silicon nanocrystals and device application // *Mater. Sci. Eng. B* **101**, p. 19-24 (2003).
7. J.A. Berashevich, B.V. Kamenev, V.E. Borisenko, Luminescence of nc-Si/dielectric multilayer structures under injection excitation // *Fizika Tekhnika Poluprovodnikov* **36** (2), p. 221-226 (2002), in Russian.
8. O.B. Gusev, M. Voydak, M. Klik, M. Forkales, T. Gregorkevich, Excitation of erbium in the SiO_2:Si-nc matrix at the impulsive pumping // *Fizika Tverdogo Tela* **47** (1), p. 105-107 (2005), in Russian.
9. V.A. Dan'ko, I.Z. Indutnyy, V.S. Lysenko, I.Yu. Maidanchuk, V.I. Min'ko, A.N. Nazarov, A.S. Tkachenko, P.E. Shepeliavyi, Kinetics of structural-phase transformations in thin SiO_x films in the course of rapid thermal annealing // *Fizika*

Tekhnika Poluprovodnikov **39** (10), p. 1239-1245 (2005), in Russian.

10. D.V. Nefedov, R.K. Yafarov, Influence of temperature on formation of silicic nanocrystallites on noncrystalline substrates in plasma of microwave gas discharge // *Zhurnal Tekhnicheskoy Fiziki* **34** (2), p. 62-68 (2007), in Russian.
11. V.Ya. Aleshkin, N.A. Bekin, M.N. Buyanova, B.N. Zvonkov, A.V. Murel, Investigation of the electron density of states in quantum wells and quantum dot arrays by $C-V$ method // *Fizika Tekhnika Poluprovodnikov* **33** (10), p. 1246-1252 (1999), in Russian.
12. A.J. Chiquito, Yu.A. Pusep, S. Mergulhao, and J.C. Galzerani, Capacitance-voltage profile in a structure with negative differential capacitance caused by the presence of InAs/GaAs self-assembled quantum dots // *Phys. Rev.* **61**, p. 5499-5504 (2000).
13. V.V. Ilchenko, A.A. Buyanin, K.Y. Panarin, S.D. Lin, N.V. Shkil, Observation of the negative differential capacitance in Schottky diodes with InAs quantum dots near room temperature // *Appl. Phys. Lett.* **90**, 263114 (1-3) (2007).
14. S.D. Lin, V.V. Ilchenko, V.V. Marin, O.O. Buyanin, K.Y. Panarin, O.V. Tretyak, Frequency dependence of negative differential capacitance in Schottky diodes with InAs quantum dots // *Appl. Phys. Lett.* **93**, 103103(1-3) (2008).
15. V.V. Ilchenko, K.Y. Panarin, A.A. Buyanin, V.V. Marin, N.V. Shkil, O.V. Tretyak, Modelling of the frequency dependence of capacitance-voltage characteristics of metal-semiconductor contact with quantum dot layer // *Zhurnal fizychnykh doslidzhen'* **12** (1), 1801(1-7) (2008), in Ukrainian.
16. G.Y. Hu, R.F. O'Connel, Y.L. He, M.B. Yu, Electronic conductivity of hydrogenated silicon films // *J. Appl. Phys.* **78** (6), p. 3945-3948 (1995).
17. A.S. Gudovskikh, J.-P. Kleider, E.I. Terukov, Characterization of a-Si:H/c-Si interface by admittance spectroscopy // *Fizika Tekhnika Poluprovodnikov* **39** (8), p. 940-944 (2005), in Russian.
18. N.F. Mott, E.A. Davis, *Electronic Processes in Non-Crystalline Materials,* 22-nd ed., vol. l. Clarendon, Oxford, 1979.
19. V.V. Ilchenko, V.V. Marin, I.M. Khacevich, Investigation of capacitance-voltage characteristics of MIS-structure with Si-nanoclusters // *Proc. 3-rd Intern. Sci. and Techn. Conf. "Sensors Electronics and Microsystems Technology" "SEMST-3",* Ukraine, Odessa, June 2-7, 2008, p. 124.